深圳市华远显示器件有限公司

SHENZHEN HUAYUAN DISPLAY CO.,LTD.

液晶显示模块规格书

Specification for Liquid Crystal Display Module

HYG1926443G-bT62L-VA

Prepared By	Reviewed By	Approved By
Date:	Date:	Date:

REVISION HISTORY

The following table tracks the history of the changes made to this document.

SN	Rev.	Content	Date	Design
1	R00	Origin Released	2011-02-18	

CONTENTS

1. 0 GENERAL DESCRIPTION

The HYG1926443G-bT62L-VA is a 132x64 dots dot-matrix LCD module. It has a STN panel composed of 192 segments and 64 commons. The LCM can be easily accessed by microcontroller via 4-wires serial interface.

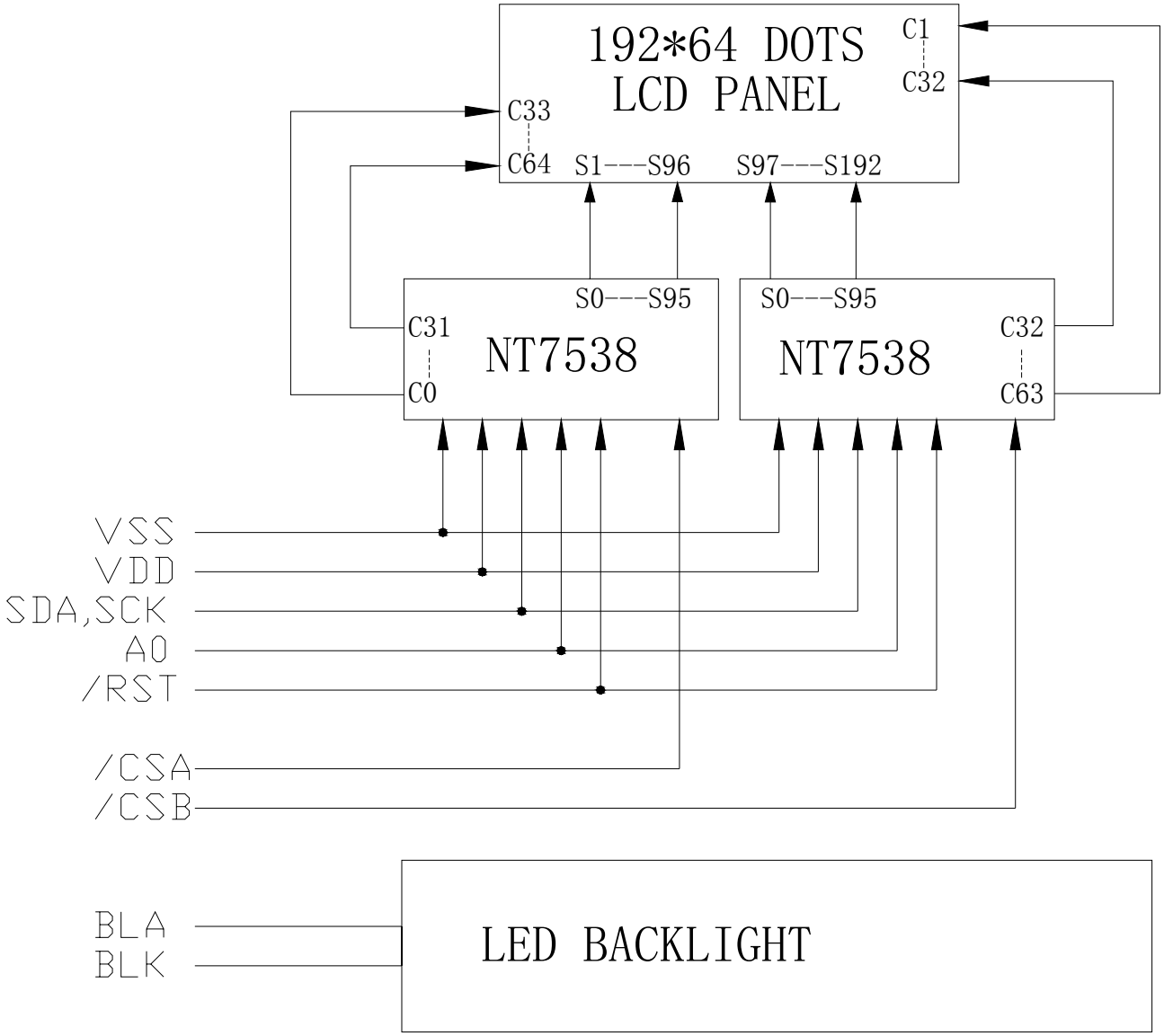
2. 0 FEATURES

Display Format	128x 64 dots
LCD Type	STN-BLUE-NEGATIVE
Polarizer Mode	TRANSMISSIVE
Drive Method	1/65 Duty, 1/9 Bias
Viewing Direction	6 O'clock
Controller	NT7538
Interface	4-wires serial interface
Backlight	Green Side-Light Type LED Backlight

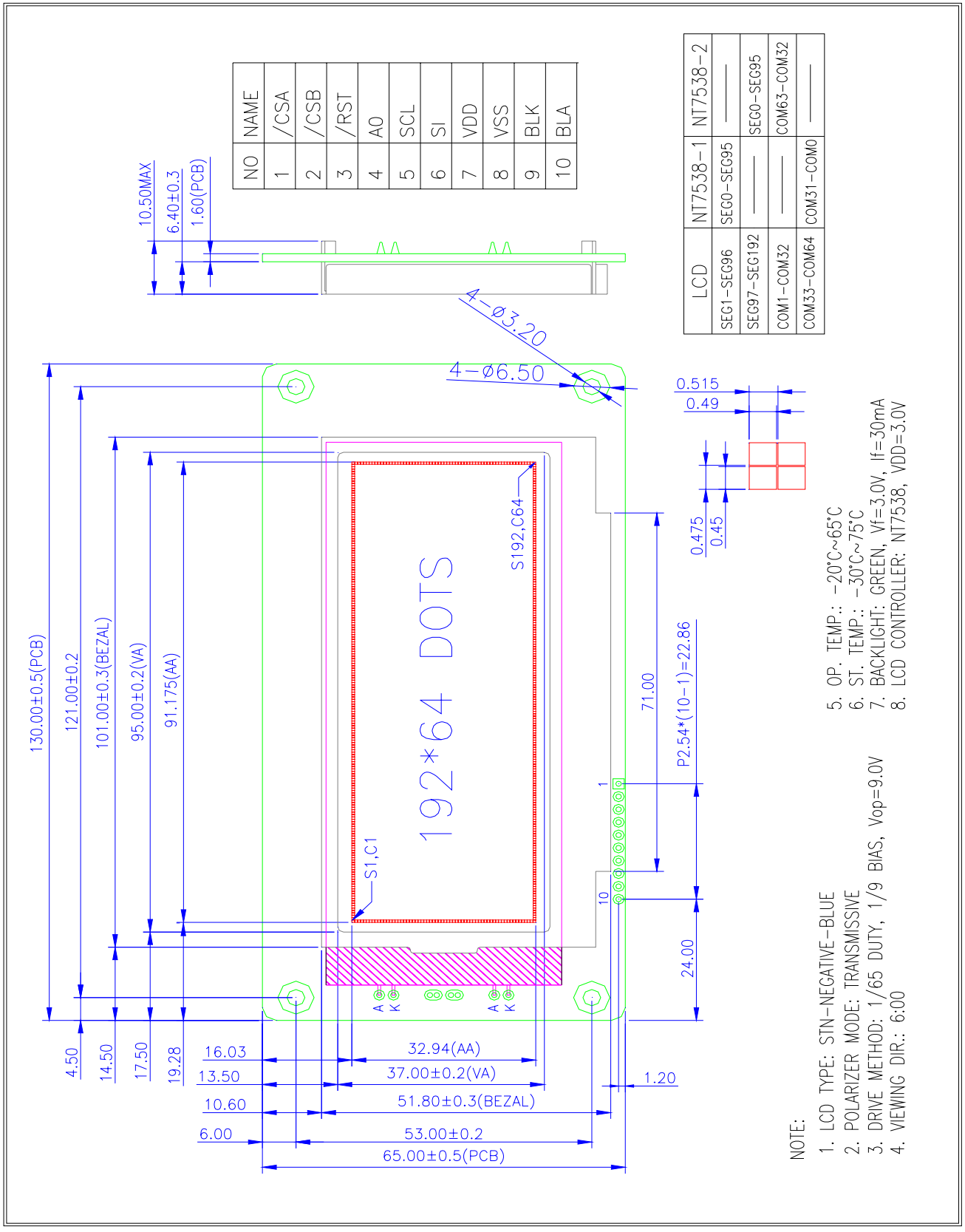
3. 0 MECHANICAL SPECIFICATION

Item	Description	Unit
Module Dimension	130.0(W) × 65.0(H) × 10.5(Max)(T)	mm
Viewing Area	95.0(W) × 37.0(H)	mm
Active Area	91.175(W) × 32.940(H)	mm
Dot Size	0.450(W) × 0.490(H)	mm
Dot Pitch	0.475(W) × 0.515 (H)	mm
Character Size	——	mm

4. 0 BLOCK DIAGRAM



5. 0 EXTERNAL DIMENSIONS



6. 0 INTERFACE PIN DESCRIPTIONS

PIN No.	Symbol	Level	Description
1	/CSA	H/L	The chip select (Left Part) signal. When /CSA = "L", then the chip select becomes active, and data/command I/O is enabled.
2	/CSB	H/L	The chip select (Right Part) signal. When /CSB = "L", then the chip select becomes active, and data/command I/O is enabled.
3	/RST	H/L	When /RES is set to "L", the settings are initialized
4	A0	H/L	It determines whether the data bits are data or command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
5	SCL	H/L	The serial clock input terminal
6	SI	H/L	The serial data input terminal
7	V_{DD}	P	Power supply for logic(+3.0V)
8	V_{SS}	P	Power Ground
9	BLK	P	Power supply for LED Backlight - (0V)
10	BLA	P	Power supply for LED Backlight + (+5.0V)

7. 0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic)	V_{DD}-V_{SS}	-0.3	4.0	V
Supply Voltage (LCD)	V_0- V_{SS}	-0.3	15.0	V
Input Voltage	VI	-0.3	V_{DD}+0.3	V
Operating Temperature	Topr	-20	+65	℃
Storage Temperature	Tstg	-30	+75	℃

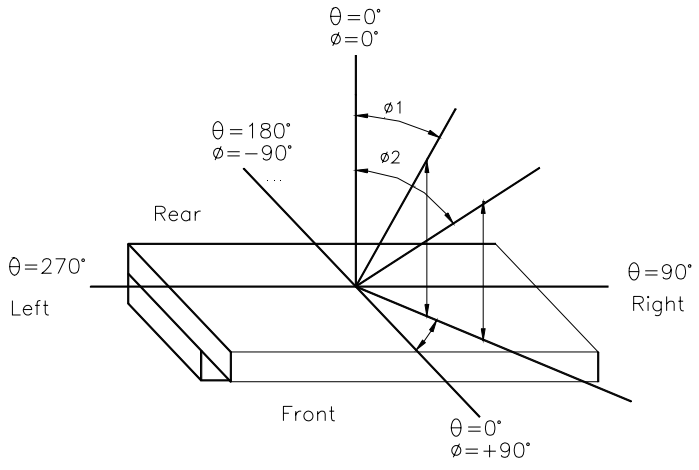
8. 0 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for Logic	V_{DD}	--	2.4	3.0	3.3	V
LCD Operating Voltage	V0-V_{SS}	-20℃				V
		+25℃	8.8	9.0	9.3	V
		+65℃				V
Input voltage H level	V_{IH}	For all inputs	0.8V_{DD}	---	V_{DD}	V
Input voltage L level	V_{IL}	For all inputs	V_{SS}	---	0.2V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = –0.5 mA	0.8V_{DD}	---	V_{DD}	V
Output Low Voltage	V_{OL}	I_{OL} = 0.5 mA	V_{SS}	---	0.2V_{DD}	V
Frame Frequency	fFRM	1/65 duty Fosc=31.4KHz	78	80	83	Hz

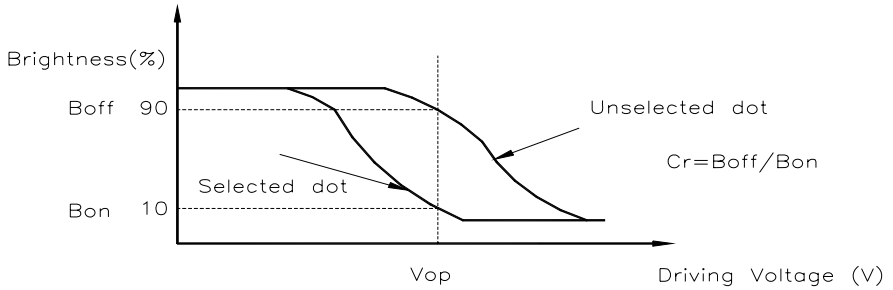
9. 0 OPTICAL CHARACTERISTICS

Item	Symbol	Condition		Min	Typ	Max	Unit
Response time	Ton	θ=0 ° and Ta=-20℃					ms
		θ=0 ° and Ta=+25℃		-			ms
		θ=0 ° and Ta=+65℃					ms
	Toff	θ=0 ° and Ta=-20℃					ms
		θ=0 ° and Ta=+25℃		-			ms
		θ=0 ° and Ta=+65℃					ms
Contrast ration	CR(MAX)	Ta=25℃		5	10		---
Viewing Angle	Ø	Deg θ=0 °	CR≥2.0 Ta=25℃		50		Deg
		Deg θ=90 °			35		
		Deg θ=180 °			30		
		Deg θ=270 °			35		
Crosstalk		Ta=25℃			1.2		---

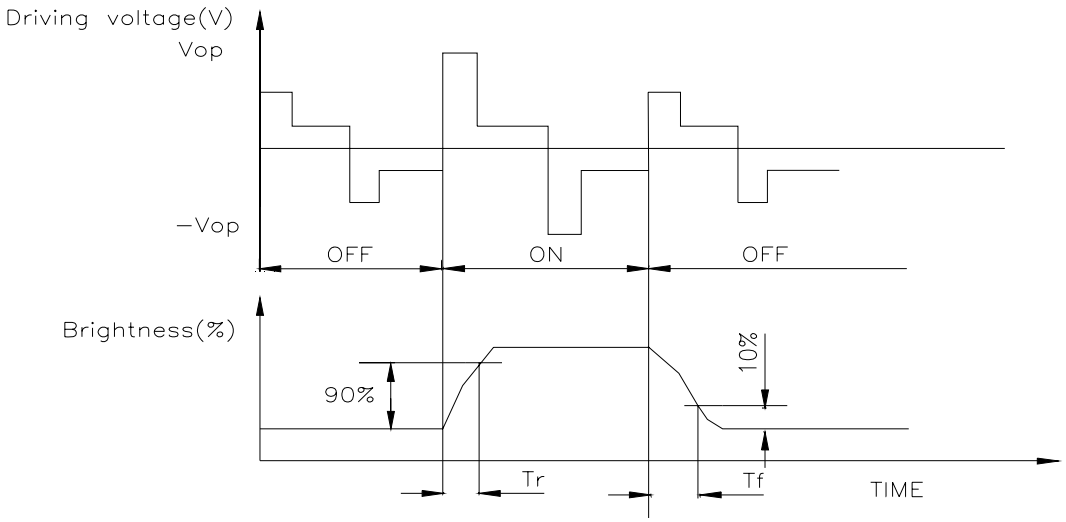
9.1 Viewing Angle θ , Ø and Viewing Angle Range:ΔØ =|Ø2-Ø1|



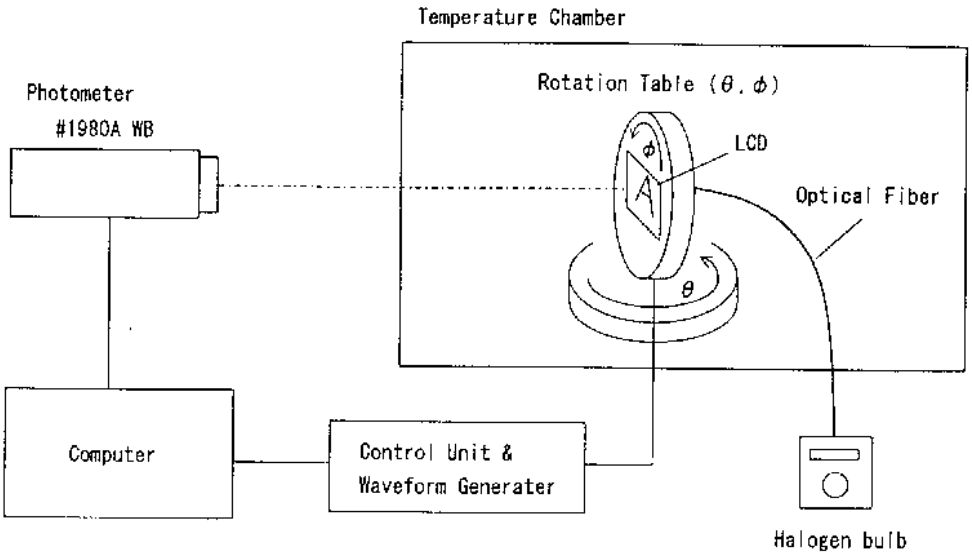
9.2 Contrast ratio(CR)



9.3 Response Time

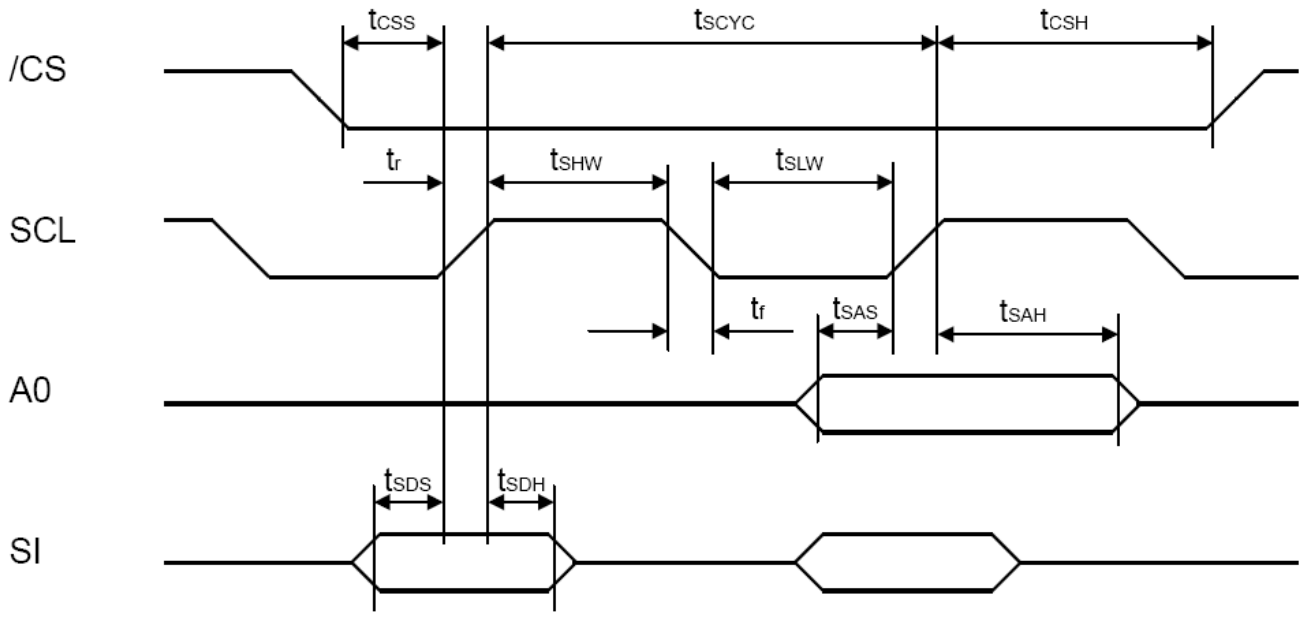


9.4 Optical Measurement System



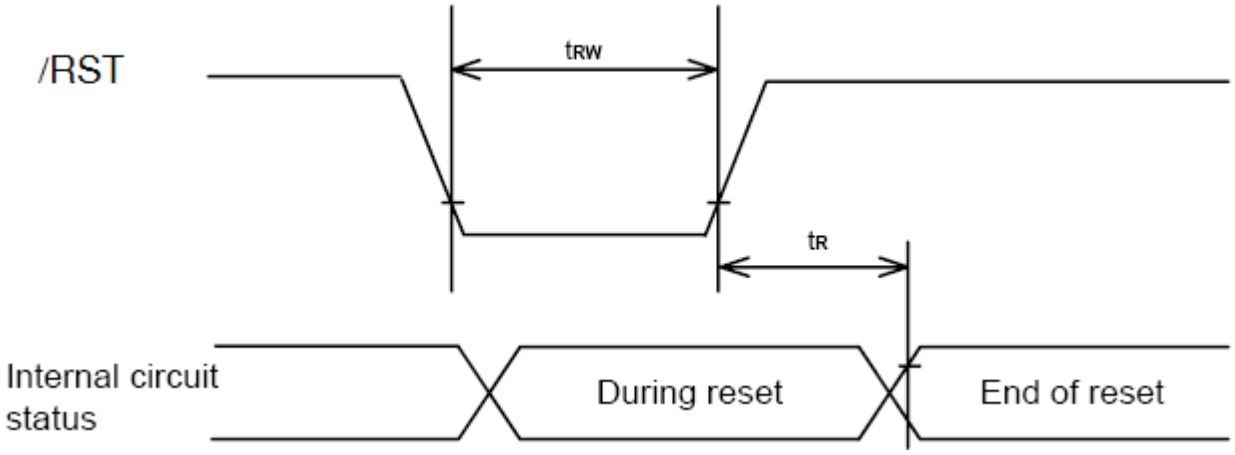
10. 0 TIMING CHARACTERICS

10.1 Serial Interface Characteristics



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tSCYC	Serial clock cycle	120			ns	SCL
tSHW	Serial clock H pulse width	60			ns	SCL
tSLW	Serial clock L pulse width	60			ns	SCL
tSAS	Address setup time	30			ns	A0
tSAH	Address hold time	20			ns	A0
tSDS	Data setup time	30			ns	SI
tSDH	Data hold time	20			ns	SI
tCSS	/CS serial clock time	20			ns	/CS
tCSH	/CS serial clock time	40			ns	/CS

10.4 Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tR	Reset time			1.0	μs	
tRW	Reset low pulse width	10			μs	/RST

11. 0 BACKLIGHT CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Item	Symbol	Condition	Rating	Unit
Reverse Voltage	Vr		5.0	V
Absolute maximum forward current	Ifm		40	mA
Forward Current	If	Vf=3.0V	30	mA
Power Description	Pd		90	mW
Operating temperature range	Topr		-20~+65	^{0}C
Storage temperature range	Tst		-30~+75	^{0}C

11.2 ELECTRICAL/OPTLCAL CHARACTERISTICS

(Ta=25℃)

Item	Symbol	Min	Typ	Max	Unit	Condition
Forward Voltage	Vf	2.8	3.0	3.2	V	If=15 mA
Reverse Current	Ir		20		uA	Vr=5.0 V
Dominant wave length	λp	--	--	--	nm	If=15 mA
Spectral Line Half width	Δλ		--			If=15 mA
Luminance	Lv				cd/㎡	If=15 mA
Color Coordinate	X		GREEN			If=15 mA
	Y					

12. 0 OPERATING PRINCIPLES & METHODS

12.1 The Serial Interface

When the serial interface has been selected (P/S = “L”), then when the chip is in an active state (/CS= “L”, the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of the eighth serial clock for processing.

The A0 input is used to determine whether or not the serial data input is displaying data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active. Figure 12-1 is the serial interface signal chart.

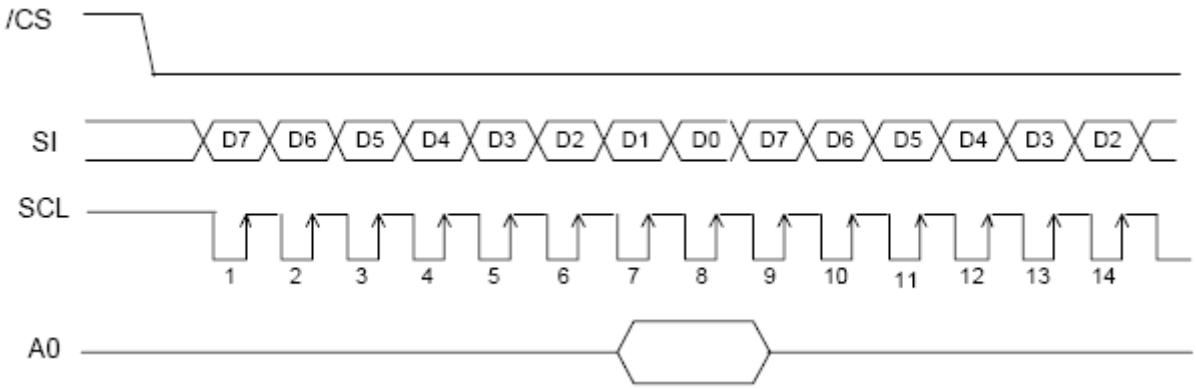


Figure 12-1

●When the chip is not active, the shift registers and the counter are reset to their initial states.

●Reading is not possible while in serial interface mode.

●Caution is required on the SCL signal as to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

12.2 Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a 65(8 page * 8 bit+1)*132 bit structure.

It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 12-2, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7538 chips are used, thus display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).

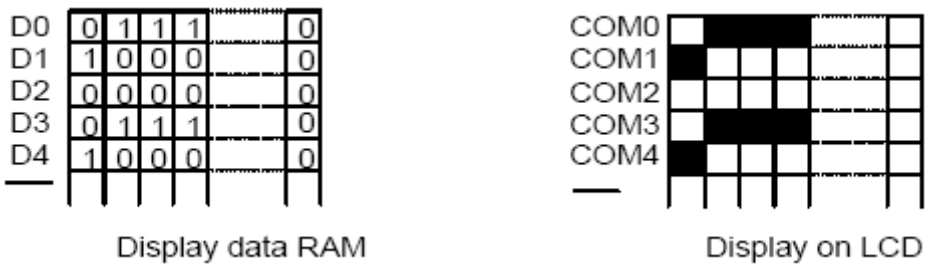


Figure 12-2

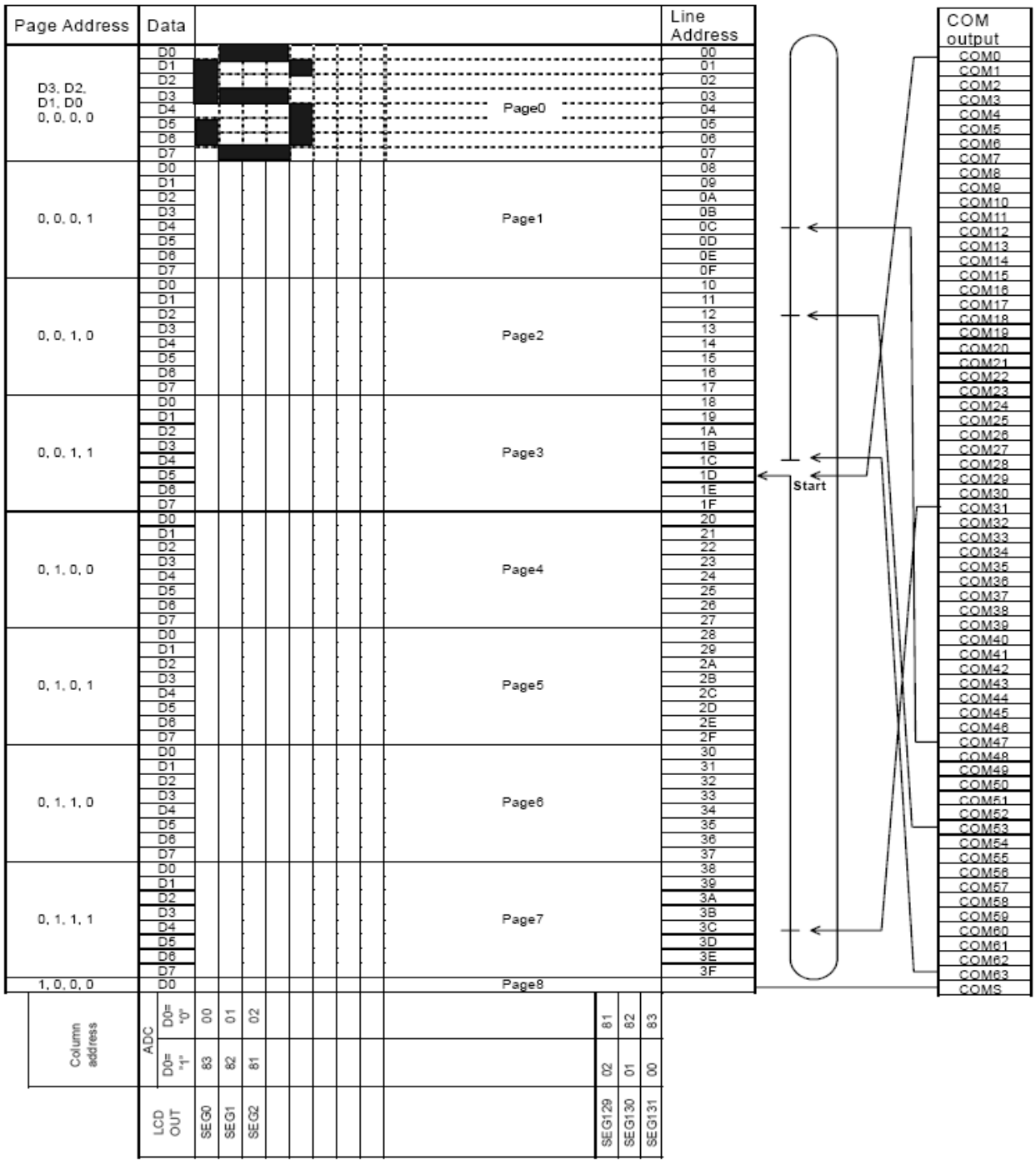


Figure 12-3

12.3 The Reset Circuit

When the /RST input falls to “L”, these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/55, 1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear: V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = “L”)
17. Output condition of COM, SEG

COM: V1

SEG: V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect. The /RST terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RST terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an over current condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7538, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an “L” signal to the /RST terminal when the external liquid crystal power supply is applied. Even though the oscillator circuit operates while the /RST terminal is “L,” the display timing generator circuit is stopped, and the FR, FRS, and /DOF terminals are fixed to “H,” and the CL pin is fixed to “H” only when the intermal oscillator circuit is used. There is no influence on the D0 to D7 terminals

12.4 The Voltage Regulator Circuit

The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7538 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

12.4.1 When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where V0 < VOUT.

V0 = (1+Rb/Ra)*VEV = (1+Rb/Ra)* (1-(63-α)/162)*VREG (Equation A-1)

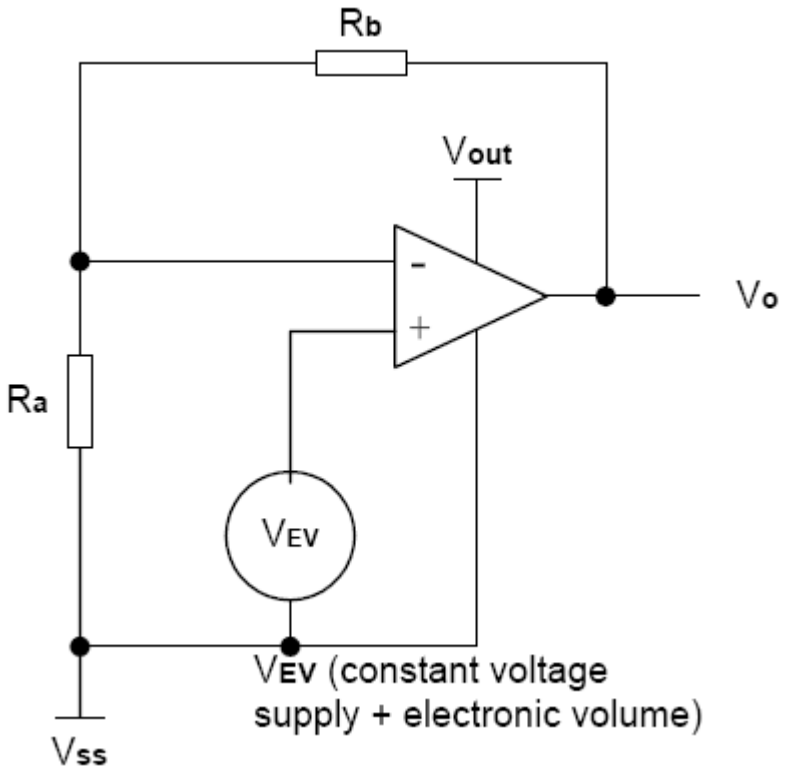


Figure 12-4

VREG is the IC internal fixed voltage supply, and its voltage at Ta = 25℃ is shown in Table 12-1

Equipment Type	Thermal Gradient	Units	VREG
Internal power Supply	-0.05	%/℃	2.1

Table 12-1

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 12-2 shows the value for α depending on the electronic volume register settings.

Ra/Rb is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 12-3 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32 (default)	:
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

Table 12-2

V0 voltage regulator internal resistance ratio register value and (1+ Rb/Ra) ratio (Reference value)

Register			Equipment Type by Thermal Gradient [Units:%/ ℃]	
D2	D1	D0	-0.05 %/℃	VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

Table 12-3

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

13. 0 INSTRUCTION DESCRIPTION

13.1 INSTRUCTION TABLE

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display on/off	0	1	0	1	0	1	0	1	1	1	0 1	Turns on the LCD panel when high, and turns it off when low
(2) Set display start line	0	1	0	0	1	Display start address						Specifies RAM display line for COM0
(3) Page address Set	0	1	0	1	0	1	1	Page address				Sets the display RAM page in Page Address register
(4) Column address Set	0	1	0	0	0	0	1	Higher column address				Sets 4 higher bits and 4 lower bits of column address of display RAM in register
	0	1	0	0	0	0	0	Lower column address				
(5) Read status	0	0	1	Status				0	0	0	0	Reads the status information
(6) Write display data	1	1	0	Write data								Writes data in display RAM
(7) Read display data	1	0	1	Read data								Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence
(9) Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Normal indication when low, but full indication when high
(10) Entire display on/off	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)
(11) Set LCD bias	0	1	0	1	0	1	0	0	0	1	0 1	Sets LCD drive voltage bias ratio
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write

续表

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions
(15) Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data
(16) Set power control	0	1	0	0	0	1	0	1	Operation status			Selects the power circuit operation mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio (Rb / Ra) mode
(18) Electronic volume mode set Electronic Volume Register set	0	1	0	1	0	0	0	0	0	0	1	Sets the V0 output voltage electronic volume register
	0	1	0	*	*	Electronic control value						
(19) Set static indicator On/Off Set Static indicator register	0	1	0	1	0	1	0	1	1	0	0 1	Sets static indicator On/Off 0: OFF 1: ON
	0	1	0	*	*	*	*	*	*	Mode		Sets the flashing mode
(20) Power save	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(22) Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	Select the oscillation frequency
(23) Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty ratio			Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias ratio			Sets the LCD bias ratio for partial display mode

续表

Command	Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	Sets the LCD Number of partial display start line
	0	1	0	1	1	Partial Start Line						
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	Sets the number of line used for N-Line inversion
	0	1	0	*	*	*	Number of Line					
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	Set DC/DC Clock frequency
	0	1	0	1	1	0	0	Clock Division				
(30) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use (F1h to FFh)
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset

13.2 DESCRIPTION OF INSTRUCTION

1) Display ON/OFF

Alternatively turns the display on and off.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, the power save mode is entered. See the section on the power saver for details.

2) Set Display Start Line

Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of the LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. This command changes when the line address, smooth scrolling or a page change take place.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4) Set Column Address

It specifies column address of display RAM. It divides the column address into 4 higher bits and 4 lower bits. Set each of them in succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental during each access until address 132 is accessed. The page address is not changed during this time.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	0	0	0	1	A7	A6	A5	A4	Higher bits
0	1	0	0	0	0	0	A3	A2	A1	A0	Lower bits

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
				:				:
1	0	0	0	0	0	1	1	131

5) Read Status

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7538 is busy due to the internal operation or reset. Any command is rejected until BUSY becomes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “131-n” corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

ADC: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates that the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is reset.

6) Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7) Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after the column address setup. Refer to the display RAM section of the FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8) ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 12-3. When display data is written or read, the column address is incremented by 1 as shown in Figure 12-3.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, rotation is to the right (normal direction)
When D is high, rotation is to the left (reverse direction)

9) Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)
When D is high, the RAM data is low, being LCD ON potential (reverse display)

10) Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11) Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

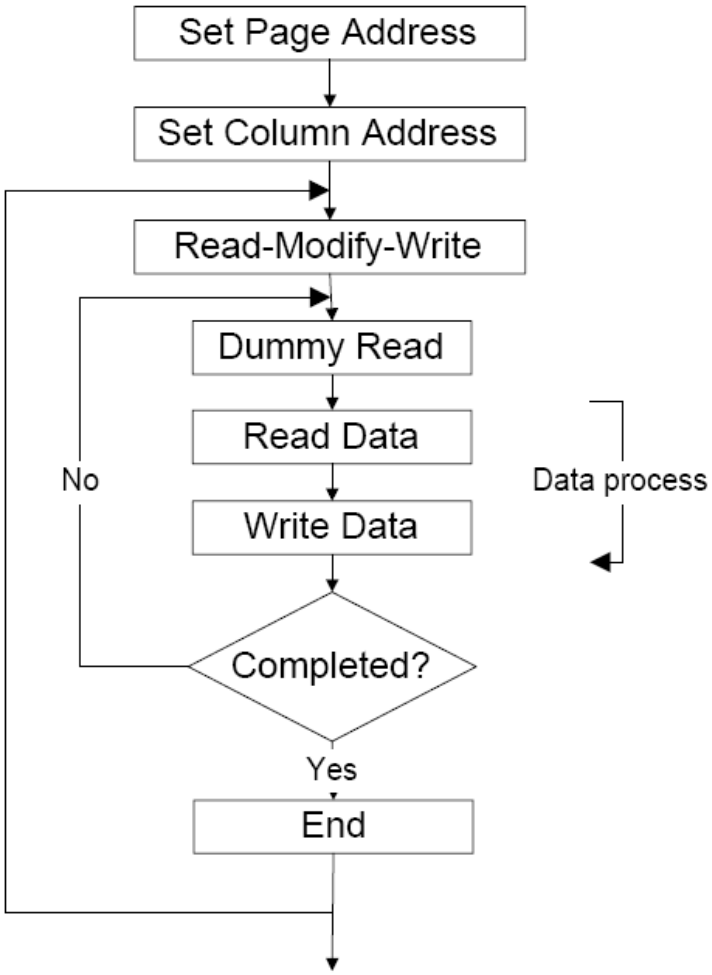
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	1	0 1	1/9 bias 1/7 bias

12) Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, the column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until the End command is issued. When the End is issued, the column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed when the cursor is blinking or other events.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

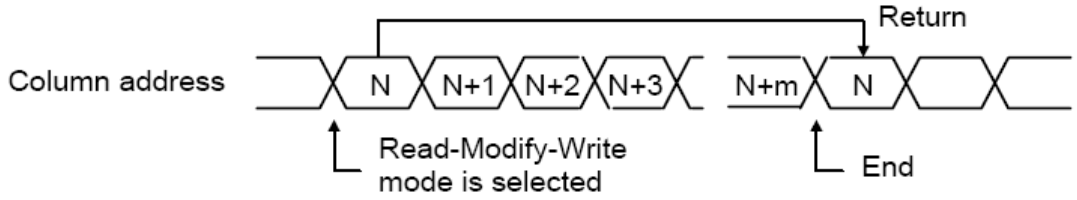
Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode



13) End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued).

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



14) Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the /RST pad can initialize the supplies.

15) Output Status Select Register

Applicable to the NT7538. When D is high or low, the scan direction of the COM output pad is selectable.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pad
D = 0: Normal (COM0 → COM63)
D = 1: Reverse (COM63 → COM0)
*: Invalid bit

16) Set Power Control

Selects one of eight-power circuit functions using a 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. R

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 is low, the voltage follower turns off. When A0 is high, it turns on.
When A1 is low, the voltage regulator turns off. When A1 is high, it turns on.
When A2 i low, the voltage booster turns off. When A2 is high, it turns on.

17) V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		:
								1	1	0	
								1	1	1	Large

18) The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.

This command is a double byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	0	Small
					0	0	0	0	0	1	
					0	0	0	0	1	0	
									:		:
					1	1	1	1	1	0	
					1	1	1	1	1	1	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19) Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator registers, and these commands must be executed one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D = 0: Static Indicator OFF

D = 1: Static Indicator ON

Static Indicator Register Set

These commands set two bits of data into the static indicator register and are used to set the static indicator into a blinking mode.

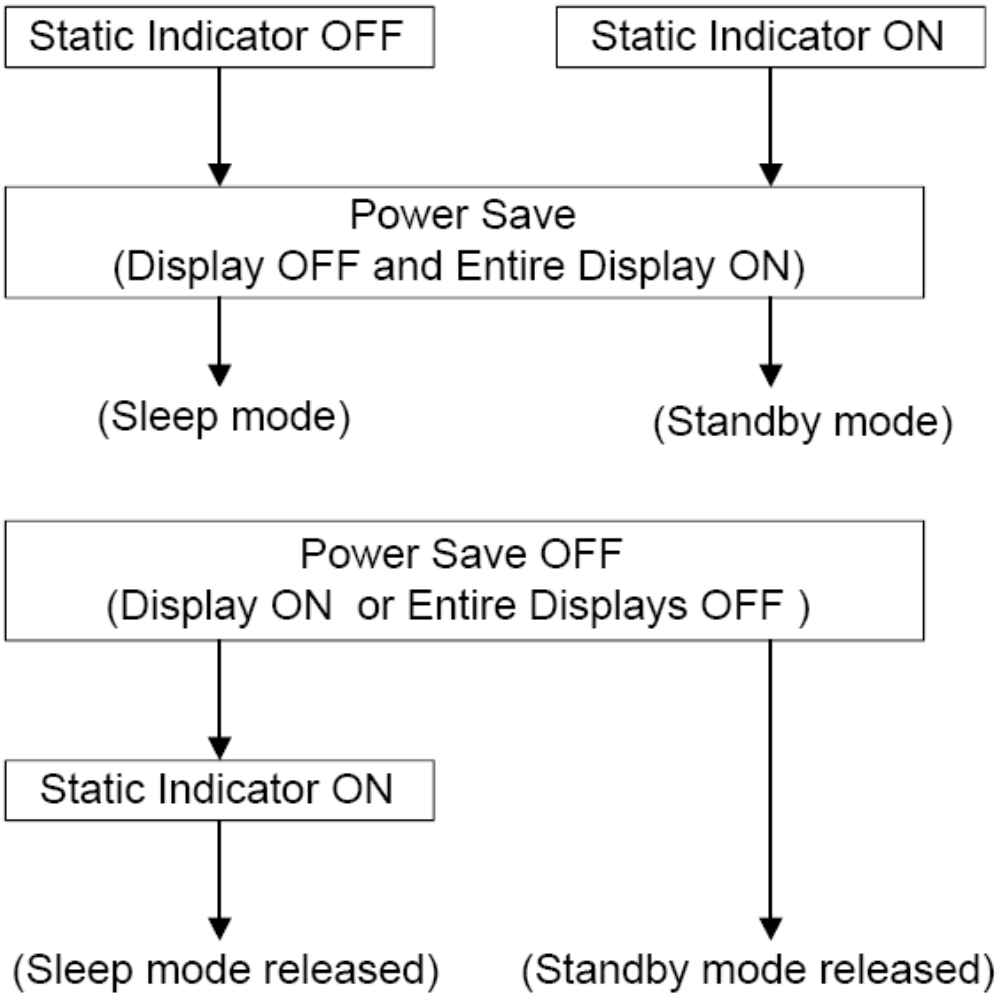
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately 0.5 second intervals
									1	0	ON (blinking at approximately 1 second intervals
									1	1	ON (constantly on)

20) Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicators are off, the Power Save command makes the system enter sleep mode. If it is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.

(2) Stops the LCD drives and outputs the VSS level as the segment/common driver output.

(3) Holds the display data and operation mode provided before the start of the sleep mode.

(4) The MPU can access the built-in display RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for the static drive.

The ON operation of the static drive system indicates that the NT7538 is in standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.

(2) Stops the LCD drive and outputs the VSS level as the segment / common driver output.

However, the static drive system still operates.

(3) Holds the display data and operation mode provided before the start of the standby mode.

(4) The MPU can access the built-in display RAM.

When the RESET command is issued in the standby mode, the sleep mode is set.

● When an external resistive driver gives the LCD driving voltage level, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go to the sleep mode or standby mode.

● When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go into sleep mode or standby mode.

21) NOP

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22) Oscillation Frequency Select

This command is to select the oscillation frequency of driver IC as below.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Oscillation Frequency
0	1	0	1	1	1	0	0	1	0	0	Typical 31.4 KHz
										1	Typical 26.3 KHz

23) Partial Display Mode Set

This command enables to select the display mode. When D0 is low, the IC is in normal display mode, the maximum display duty ratio is decided by pin connection of DUTY0 and DUTY1 and the command LCD Bias Set decides the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set decide the LCD display duty and bias ratios.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Display Mode
0	1	0	1	0	0	0	0	0	1	0	Normal Display
										1	Partial Display

24,25) Partial Display Duty and Bias Set

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. They are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is set simultaneous as below. The partial display duty will be kept at maximum duty (decided by pins DUTY0 and DUTY1) when setting duty is larger than maximum duty.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	1/9 duty	Line [0:7], COMS
								0	0	1	1/17 duty	Line [0:15], COMS
								0	1	0	1/33 duty	Line [0:31], COMS
								0	1	1	1/49 duty	Line [0:47], COMS
								1	0	0	1/65 duty	Line [0:63], COMS
								1	0	1	Reserved	No effect
								1	1	*	Reserved	No effect

Using Partial Display Bias Set command to change the LCD bias in partial display mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	1/4
								0	0	1	1/5
								0	1	0	1/6
								0	1	1	1/7
								1	0	0	1/8
								1	0	1	1/9
								1	1	0	Reserved
								1	1	1	Reserved

Note: The COM waveform of no display area is non-select waveform.

26) Prtial Start Line Set (Double Byte Command)

This command makes it possible to set the partial start line for partial display. It is a two-byte command used as a pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

(1) Partial Start Line Set

When this command is input, no other command except for the Number of Start Line Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0	0	1	1

(2) Number of Start Line Set

By using this command to set six bits of data to the Partial Start Line register. Once the Number of the Start Line Set command has been used to set data into the register, then the partial start line will affect on the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than maximum duty ratio (decided by pins DUTY0 and DUTY1).

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	0 Line
					0	0	0	0	0	1	1 Line
					0	0	0	0	1	0	2 Line
								:			:
					1	1	1	1	1	0	62 Line
					1	1	1	1	1	1	63 Line

27) The N-Line Inversion (Double Byte Command)

This command makes it possible to adjust the number of scan lines for liquid crystal display inversion. It is a two-byte command used as a pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

(1) N-Line Inversion Set

When this command is input, no other command except for the Number of Line Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	1

(2) Number of Line Set

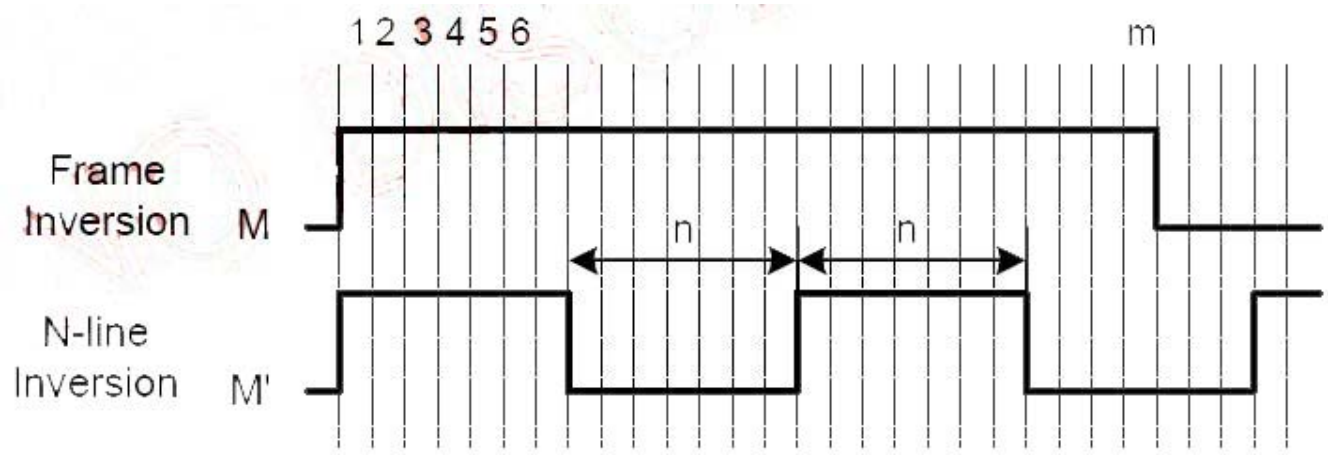
By using this command to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been used to set the data into the register, then the N-Line inversion will affect on the

LCD display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Line Inversion
0	1	0	*	*	*	0	0	0	0	0	1 Line
						0	0	0	0	1	2 Line
								:			:
						1	1	1	1	0	31 Line
						1	1	1	1	1	32 Line

Note 1: The number of inversed scan line = register setting value + 1.

Note 2: When Partial Duty = 1/9 or 1/17, the N-line inversion function release and the LCD display scan line is back to frame inversion status.



28) Release N-Line Inversion

This command is used to exit the N-Line inversion function. The N-Line inversion function is released and the LCD display is set back to frame inversion status once this command is executed.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	1	0	0

29) DC/DC Clock Frequency (Double Byte Command)

This command makes it possible to adjust the frequency for DC/DC clock. It is a two-byte command used as a pair and the DC/DC Frequency Division Set command must be issued after the DC/DC Clock Set command.

(1) DC/DC Clock Set

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	1	0

(2) DC/DC Frequency Division Set

By using this command to set five bits of data to the frequency division register.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Division
0	1	0	1	0	0	0	0	0	0	0	fOSC
							0	0	0	1	fOSC/2
							0	0	1	0	fOSC/4
							0	0	1	1	fOSC/6 (default)
							0	1	0	0	fOSC/8
							0	1	0	1	fOSC/10
							0	1	1	0	fOSC/12
							0	1	1	1	fOSC/14
							1	0	0	0	fOSC/16
							1	0	0	1	fOSC/18
							1	0	1	0	fOSC/20
							1	0	1	1	fOSC/22
							1	1	0	0	fOSC/24
							1	1	0	1	fOSC/26
							1	1	1	0	fOSC/28
							1	1	1	1	fOSC/30

30,31) Test Command

This is the dedicated IC chip test command. It must not be used for normal operation.

If the Test command is issued inadvertently set the /RST input to low or issue the Reset command to release the test mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

Cautions:

The NT7538 maintains an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

14. 0 QUALITY GUARANTEE

14.1 ACCEPTABLE QUALITY LEVEL

Inspection items	Sampling procedures	AQL
Visual-operating (Electro-optical)	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	0.65
Visual-not operating	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5
Dimension measurement	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5

14.2 Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20 25℃ and normal humidity 60 15RH).

- Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

- Driving voltage

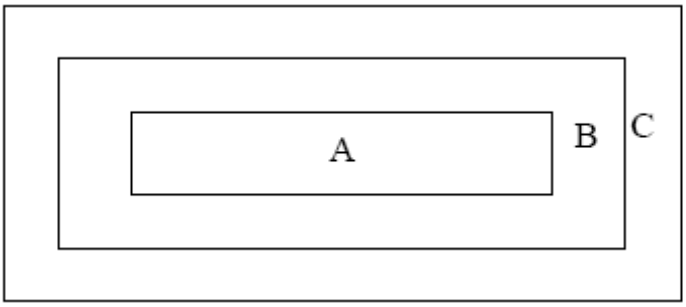
The V0 value which the most optimal contrast can be obtained near the specified V0 in the specification. (Within ±0.5V of the typical value at 25℃.).

14.3 Definition of inspection zone in LCD

Zone A: character/Digit area

Zone B: viewing area except Zone A (ZoneA+ZoneB=minimum Viewing area)

Zone C: Outside viewing area (invisible area after assembly in customer's product)



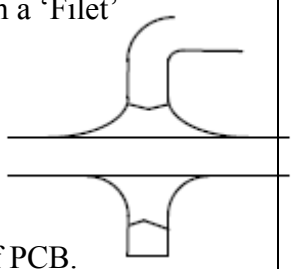
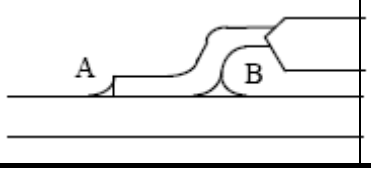
Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

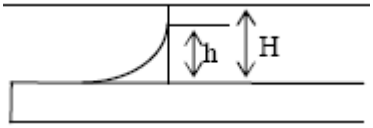
14.4 Inspection Standard

- **Major Defect**

Item No	Items to be inspected	Inspection Standard	Classification of defects
1	All functional defects	1) No display 2) Display abnormally 3) Missing vertical，horizontal segment 4) Short circuit 5) Back-light no lighting, flickering and abnormal lighting.	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed.	

- **Module Cosmetic Criteria**

No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (∅0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ∅0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a ‘Filet’ all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side (In case of ‘Through Hole PCB’) Solder to reach the Components side of PCB. 	Minor
	2. Flat packages	Either ‘Toe’ (A) or ‘Seal’ (B) of the lead to be covered by ‘Filet’. Lead form to be assume over solder. 	Minor

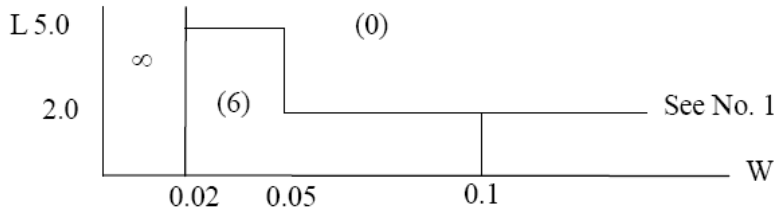
No.	Item	Judgment Criterion	Partition
8	3. Chips	(3/2) H ≥ h ≥ (1/2) H 	Minor

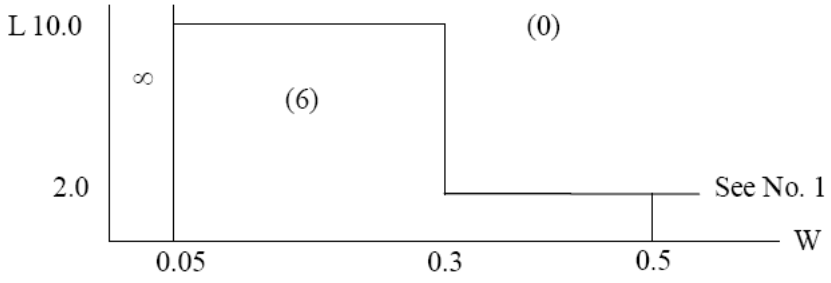
● Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition
1	Spots	In accordance with *Screen Cosmetic Criteria (Operating) No.1*.	Minor
2	Lines	In accordance with *Screen Cosmetic Criteria (Operating) No.2*.	Minor
3	Bubbles in polarizer	<table><tr><td>Size : d</td><td>mm</td><td>Acceptable Qty in active area</td></tr><tr><td>d</td><td>≤ 0.3</td><td>Disregard</td></tr><tr><td>0.3 < d</td><td>≤ 1.0</td><td>3</td></tr><tr><td>1.0 < d</td><td>≤ 1.5</td><td>1</td></tr><tr><td>1.5 < d</td><td></td><td>0</td></tr></table>	Minor
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor
7	Contamination	Not to be noticeable.	Minor

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating)

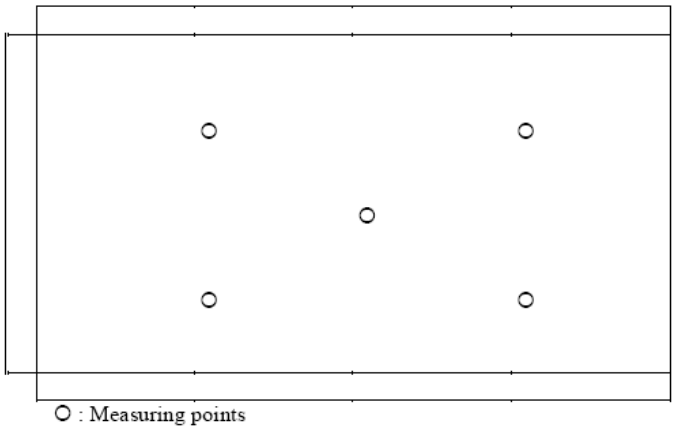
<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.1</td><td>Disregard</td></tr>
<tr><td>0.1 < d ≤ 0.2</td><td>6</td></tr>
<tr><td>0.2 < d ≤ 0.3</td><td>2</td></tr>
<tr><td>0.3 < d</td><td>0</td></tr>
</table>
Note : Including pin holes and defective dots which must be within one pixel size.
B) Unclear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.2</td><td>Disregard</td></tr>
<tr><td>0.2 < d ≤ 0.5</td><td>6</td></tr>
<tr><td>0.5 < d ≤ 0.7</td><td>2</td></tr>
<tr><td>0.7 < d</td><td>0</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>A) Clear
 

Note :
( ) - Acceptable Qty in active area
L - Length (mm)
W - Width (mm)
∞ - Disregard
B) Unclear
 

‘Clear’ = The shade and size are not changed by Vop.
‘Unclear’ = The shade and size are changed by Vop.</td><td>Minor</td></tr>
</table>

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	Minor
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as pot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤ 2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  	Minor

Note :

(1) The limit samples for each item have priority.

(2) Complex defects are defined item by item, but if the numbers of defects are defined in above table, the total number should not exceed 10.

(3) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allowed. Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of Æ5mm.
- 10 or over defects in circle of Æ10mm.
- 20 or over defects in circle of Æ20mm.

15. 0 RELIABILITY

15.1 Content of Reliability Test

No.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage	+75℃±2℃/200 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
2	Low Temperature Storage	-30℃±2℃/200 hours	
3	High Temperature Operating	+65℃±2℃/120 hours	
4	Low Temperature Operating	-20℃±2℃/120 hours	
5	Temperature Cycle	-20℃±2℃~25~+65℃±2℃×10cycles (30min.) (5min.) (30min.)	
6	High Temperature / Humidity operation	50℃±5℃×90%RH/120 hours	
7	Vibration Test	Frequency：10Hz~55Hz~10Hz Amplitude：1.5mm, X，Y，Z direction for total 3hours (Packing condition)	
8	Drooping test	Drop to the ground from 1m height, one time, and every side of carton. (Packing condition)	
9	Static electricity test	Voltage:±8KV R: 330Ω C: 150pF Air discharge, 10time	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

16. 0 PRECAUTIONS FOR USING LCD MODULES

16.1 Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketone
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

16.2 Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

16.3 Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

17. 0 USING LCD MODULES

17.1 About Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

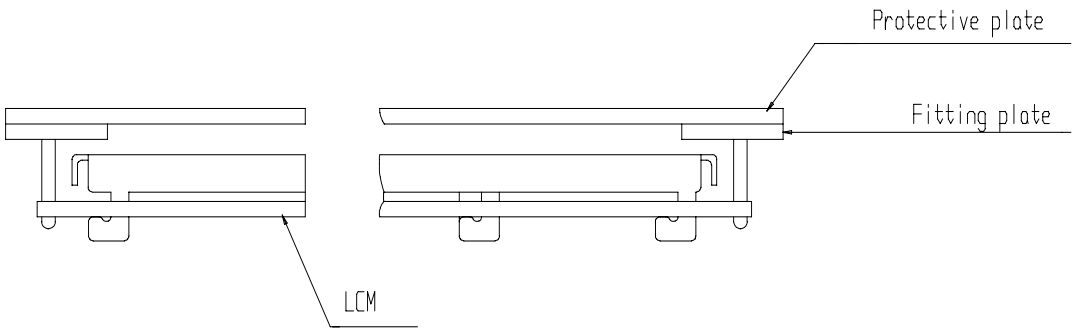
(9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinate to the polarizer).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

17.2 Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the

individual specifications for measurements. The measurement tolerance should be ±0.1mm.

17.3 Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutation of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

17.4 Soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280°C ± 10°C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

17.5 Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

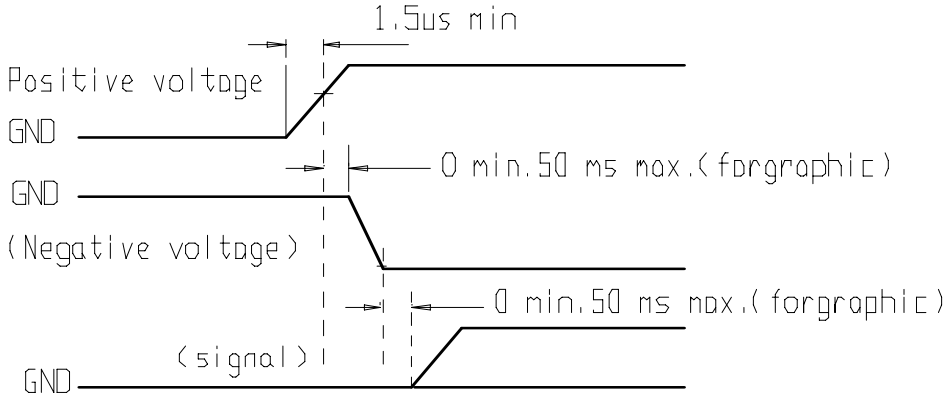
(2) Driving the LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40°C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



17.6 Storage

When storing LCDs as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

(4) Environmental conditions :

- Do not leave them for more than 168hrs. at 60°C.
- Should not be left for more than 48hrs. at -20°C.

17.7 Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

17.8 Limited Warranty

Unless agreed between HYDISPLAY and customer, HYDISPLAY will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with HYDISPLAY LCD/LCM acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to HYDISPLAY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of HYDISPLAY limited to repair and/or replacement on the terms set forth above. HYDISPLAY will not be responsible for any subsequent or consequential events.

17.9 Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet, conductors and terminals.

18. 0 APPENDIX

18.1 Initialization Code

```
void SendBit(uchar uc_dat,uchar uc_bitcnt)
{
    uchar uc_counter;
    SCK_PORT = 1;
    _nop_();
    _nop_();
    for(uc_counter=0;uc_counter<uc_bitcnt;uc_counter++)
    {
        if(( uc_dat & 0x80 ) == 0)
            SID_PORT = 0;
        else
            SID_PORT = 1; //发送数据由高位到低位传送
        _nop_();
        _nop_();
        SCK_PORT = 0; /
        _nop_();
        _nop_();
        SCK_PORT = 1;
        _nop_();
        _nop_();
        uc_dat =uc_dat <<1; //发送数据左移一位
    }
}

void wr_dat(uchar uc_dat) //Write Diaply data
{
    LCD_A0 = 1;
    _nop_();
    _nop_();
    SendBit(uc_dat,8);
    _nop_();
    _nop_();
    delay(10);
}
```

```
void wr_cmd(uchar uc_cmd) //Write Instruction Data
{
    LCD_A0 = 0;
    _nop_();
    _nop_();
    SendBit(uc_cmd,8);

    delay(10);
}

void Initialization ()
{
     LCD_CSA =0;
     LCD_CSB =0;

     wr_cmd(0xE2);    // Internal Reset

     wr_cmd(0xAE); // Display OFF

     wr_cmd(0xA0); // Set The DDRAM Address SEG output Correspondence (ADC=0)

     wr_cmd(0xC8); // Set COM Output scan direction (SHL=1)

     wr_cmd(0x40); // The DDRAM Display Start Line Address (0)

     wr_cmd(0xA6); // Set The LCD Display(Normal)
     wr_cmd(0xA2); // Set The LCD Display Driver Voltage Bias Ratio (1/9)
     wr_cmd(0xAC); // Set Static Indicator Mode = ON
     wr_cmd(0x00);

     wr_cmd(0xF8); // Set Booster Ratio (4X)
     wr_cmd(0x00);

     wr_cmd(0x2F); // Booster Circuit ON,Voltage Regulator Circuit ON,Voltage Follower Circuit ON

     wr_cmd(0x27); // Select internal resistor ratio(Rb/Ra) mode

     wr_cmd(0x81); // Set Electronic volume Register (32)
     wr_cmd(0x28);

     wr_cmd(0xAF); // Display ON

}
```

18.2 Power Supply Circuit Diagram