深圳市华远显示器件有限公司

SHENZHEN HUAYUAN DISPLAY CO.,LTD.

液晶显示模块规格书

Specification for Liquid Crystal Display Module

HYG32024032T-bT62L-VA

Prepared By	Reviewed By	Approved By
Date:	Date:	Date:

REVISION HISTORY

The following table tracks the history of the changes made to this document.

SN	Rev.	Content	Date	Design
1	R00	Origin Released	2011-12-30	

CONTENTS

1. 0 GENERAL DESCRIPTION

The HYG32024032T-bT62L-VA is a 320x240 dots dot-matrix LCD module. It has a STN panel composed of 320 segments and 240 commons. The LCM can be easily accessed by microcontroller via 8080 series interface.

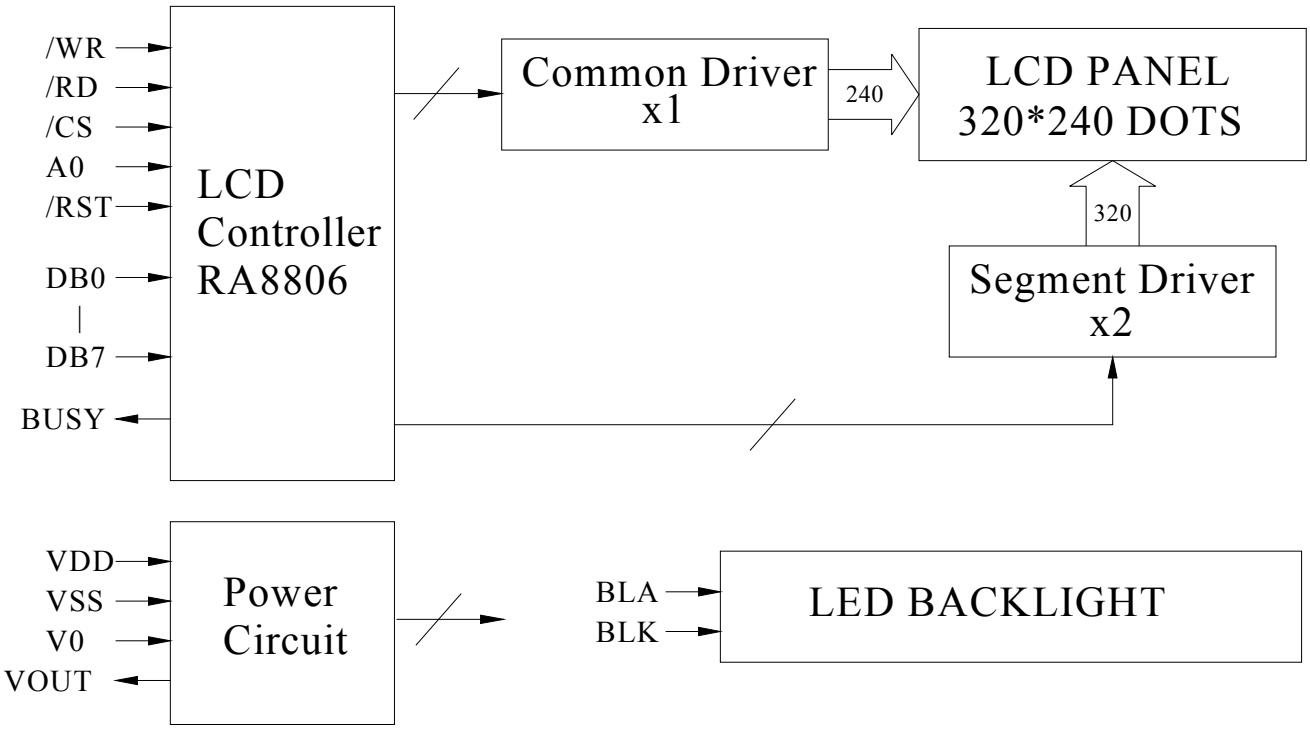
2. 0 FEATURES

Display Format	320 x 240 dots
LCD Type	STN-BLUE-NEGATIVE
Polarizer Mode	TRANSMISSIVE
Drive Method	1/240 Duty, 1/16 Bias
Viewing Direction	6 O'clock
Controller	RA8806L2N-S
Interface	8080 Series 8-Bit Parallel Interface
Backlight	White LED Backlight

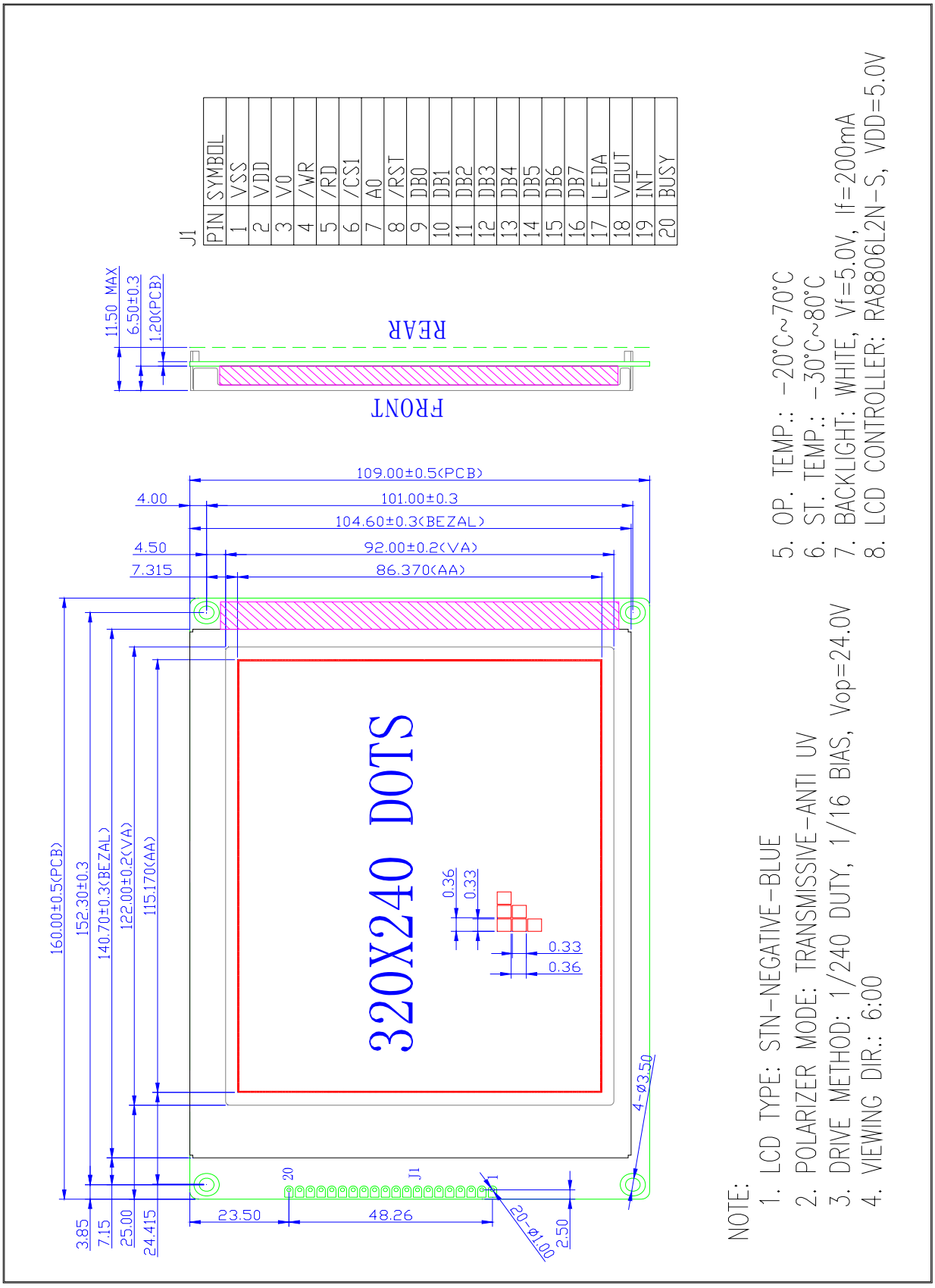
3. 0 MECHANICAL SPECIFICATION

Item	Description	Unit
Module Dimension	160.0(W) × 109.0(H) × 11.5(Max)(T)	mm
Viewing Area	122.0(W) × 92.0(H)	mm
Active Area	115.17(W) × 86.37(H)	mm
Dot Size	0.33(W) × 0.33(H)	mm
Dot Pitch	0.36(W) × 0.36(H)	mm
Character Size	——	mm

4. 0 BLOCK DIAGRAM



5. 0 EXTERNAL DIMENSIONS



6. 0 INTERFACE PIN DESCRIPTIONS

PIN No.	Symbol	Level	Description
1	V_{SS}	P	Ground
2	V_{DD}	P	Power supply for logic(+5.0V)
3	V0	P	Power supply for LCD
4	/WR	H/L	**Write Control.** This signal acts as the active-LOW.
5	/RD	H/L	**Read Control.** This signal acts as the active-LOW.
6	/CS	H/L	**Chip Select.** This signal acts as the active-LOW.
7	A0	H/L	**Register/Memory Select** The MPU will access Register when A0 is Low and access Data Memory when A0 is High.
8	/RST	H/L	**Reset Signal** This is a reset signal used to reset RA8803, Active low.
9	DB0	H/L	Data bit 0
10	DB1	H/L	Data bit 1
11	DB2	H/L	Data bit 2
12	DB3	H/L	Data bit 3
13	DB4	H/L	Data bit 4
14	DB5	H/L	Data bit 5
15	DB6	H/L	Data bit 6
16	DB7	H/L	Data bit 7
17	BLA	P	Power supply for LED Backlight (+5.0V)
18	VOUT	P	Built-in DC-DC Voltage Output (+27.0V)
19	INT	H/L	**Interrupt Signal** This is an interrupt output to indicate the status of RA8822. It could be setup active high or low.
20	BUSY	H/L	**Busy Signal** This is a busy output to indicate the RA8803 is in busy state. It could be setup active high or low.

7. 0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic)	V_{DD}-V_{SS}	-0.3	6.5	V
Supply Voltage (LCD)	V_0- V_{SS}	--	27.0	V
Input Voltage	VI	-0.3	V_{DD}+0.3	V
Operating Temperature	Topr	-20	+70	℃
Storage Temperature	Tstg	-30	+80	℃

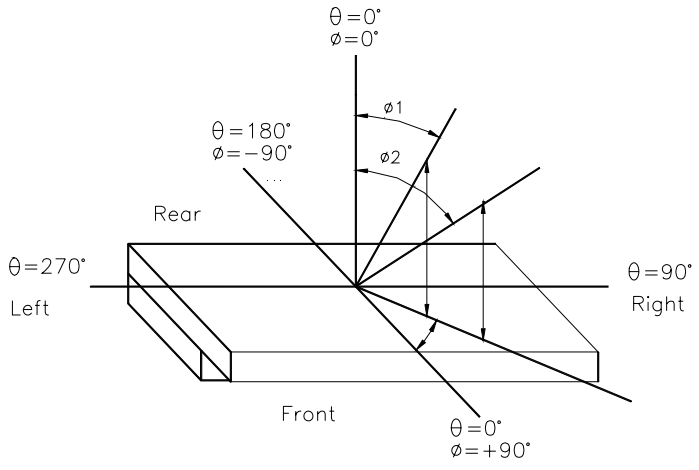
8. 0 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for Logic	V_{DD}	--	4.8	5.0	5.2	V
LCD Operating Voltage	V0-V_{SS}	-20℃				V
		+25℃	23.8	24.0	24.3	V
		+70℃				V
Input voltage H level	V_{IH}		0.8V_{DD}	--	V_{DD}	V
Input voltage L level	V_{IL}		V_{SS}	--	0.2V_{DD}	V
Output High Voltage	V_{OH}		V_{DD} -0.4	--	V_{DD}	V
Output Low Voltage	V_{OL}		V_{SS}	--	V_{DD} +0.4	V
Operation Current	I_{OPR}		1	5	10	mA

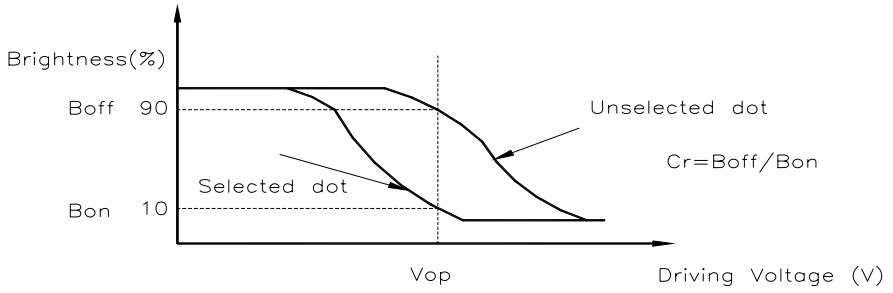
9. 0 OPTICAL CHARACTERISTICS

Item	Symbol	Condition		Min	Typ	Max	Unit
Response time	Ton	θ=0 ° and Ta=-20℃			--		ms
		θ=0 ° and Ta=+25℃		-	--		ms
		θ=0 ° and Ta=+70℃			--		ms
	Toff	θ=0 ° and Ta=-20℃			--		ms
		θ=0 ° and Ta=+25℃			--		ms
		θ=0 ° and Ta=+70℃			--		ms
Contrast ration	CR(MAX)	Ta=25℃		5	10		---
Viewing Angle	Ø	Deg θ=0 °	CR≥2.0 Ta=25℃		50		Deg
		Deg θ=90 °			35		
		Deg θ=180 °			30		
		Deg θ=270 °			35		
Crosstalk		Ta=25℃			1.2		---

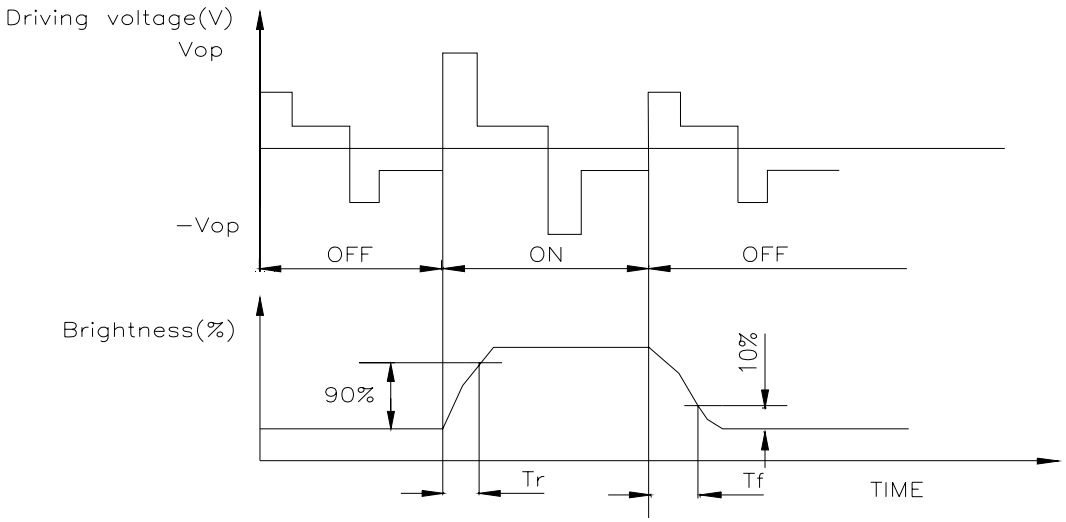
9.1 Viewing Angle θ , Ø and Viewing Angle Range: Δ Ø =|Ø2-Ø1|



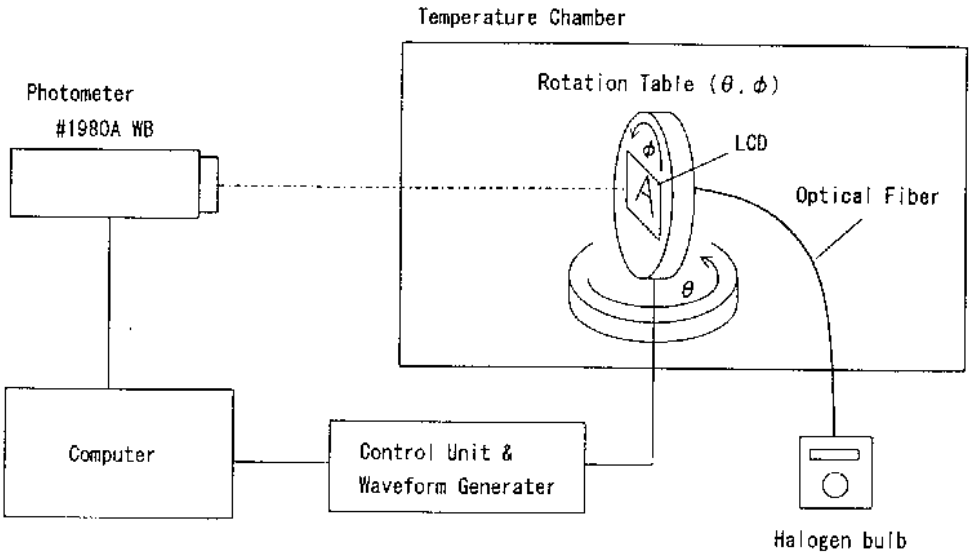
9.2 Contrast ratio(CR)



9.3 Response Time



9.4 Optical Measurement System



10. 0 TIMING CHARACTERICS

10.1 MPU Interface of 8080 Series

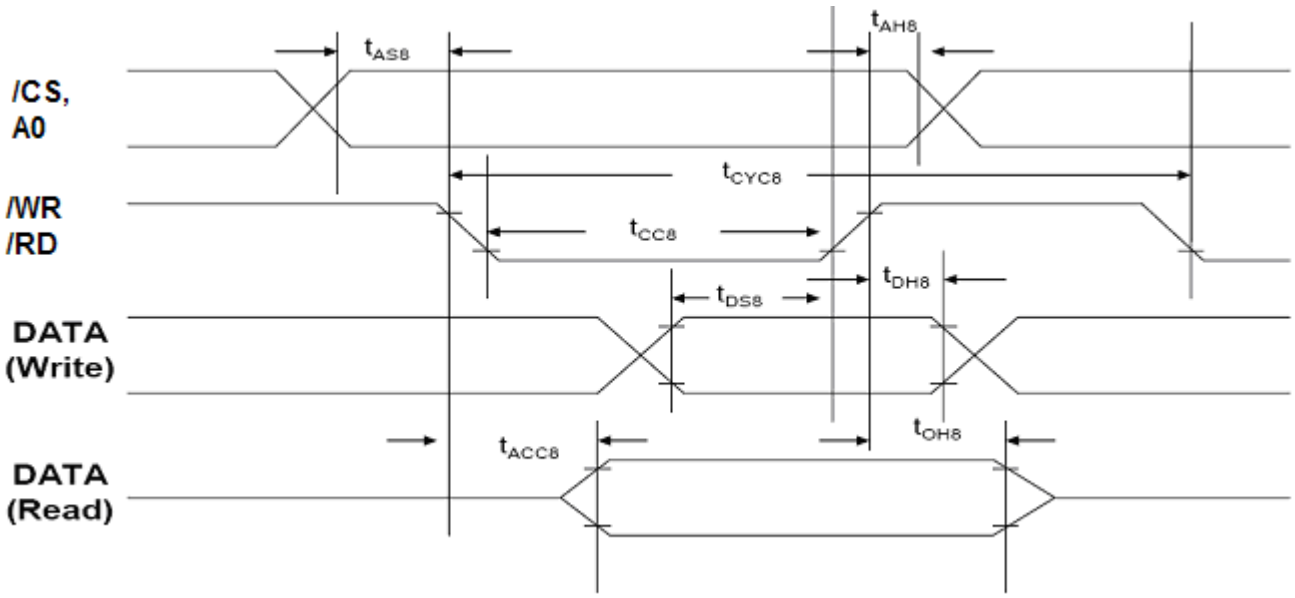


Figure 10-1：8080 MPU Interface Waveform

Symbol	Description	Rating		Unit	Condition
		Min.	Max.		
tCYC8	Cycle time	2*tc	--	ns	tc = one system clock period
tCC8	Strobe Pulse width	50	--	ns	
tAS8	Address setup time	0	--	ns	
tAH8	Address hold time	20	--	ns	
tDS8	Data setup time	30	--	ns	
tDH8	Data hold time	20	--	ns	
tACC8	Data output access time	0	20	ns	
tOH8	Data output hold time	0	10	ns	

10.2 MPU Interface of 6800 Series

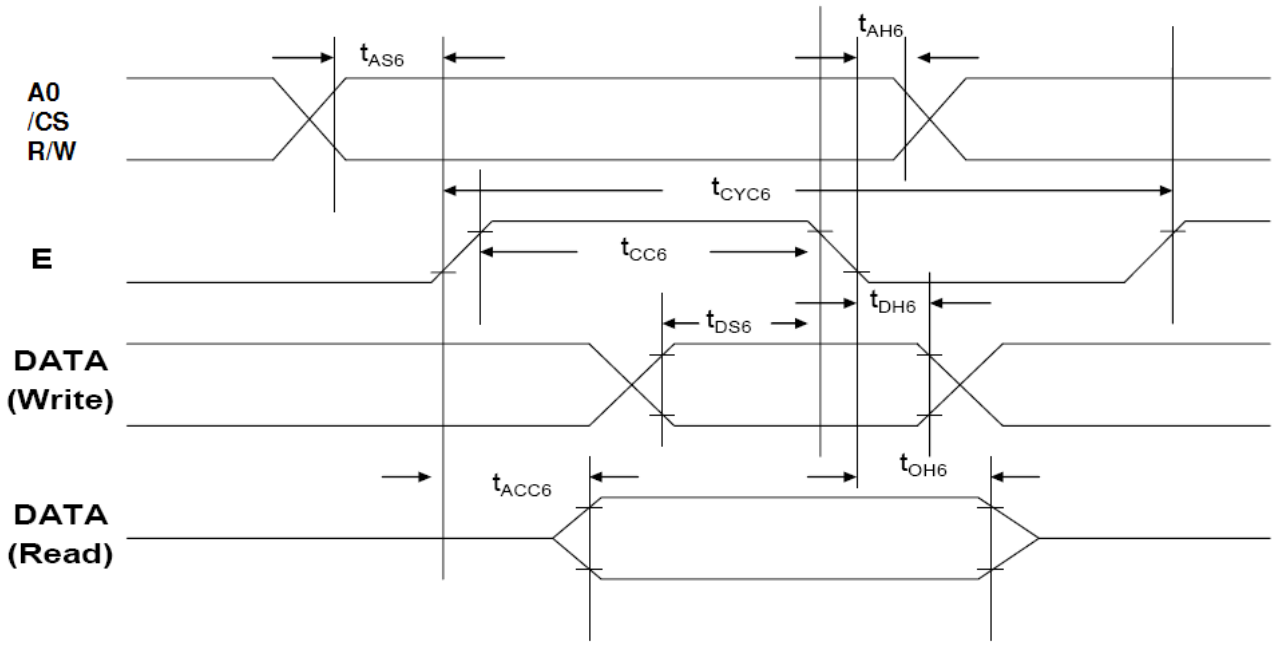


Figure 10-2：6800 MPU Interface Waveform

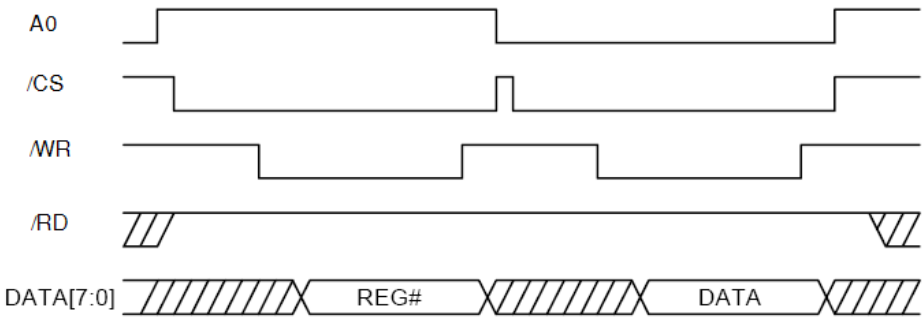
Symbol	Description	Rating		Unit	Condition
		Min.	Max.		
tCYC6	Cycle time	2*tc	--	ns	tc is one system clock period: tc = 1/CLK
tCC6	Strobe Pulse width	50	--	ns	
tAS6	Address setup time	0	--	ns	
tAH6	Address hold time	20	--	ns	
tDS6	Data setup time	30	--	ns	
tDH6	Data hold time	20	--	ns	
tACC6	Data output access time	0	20	ns	
tOH6	Data output hold time	0	10	ns	

10-3 Command Write

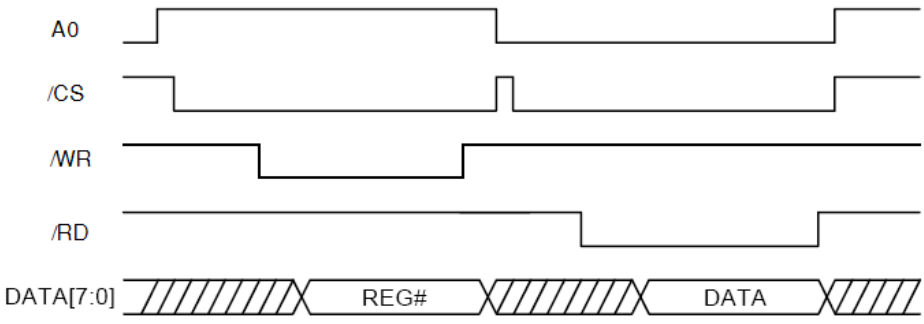
If users want to write command to RA8806, then a Command cycle has to execute first, and then execute a Data Write cycle. The “Command Write” means write function data to register. After these two cycles, the Data will write into the indicative Register. Please see the following Figure 10-3 (1).

Each command of RA8806 is take 2 cycles, and the minimum cycle time is 2*tc. So totally the minimum time of command write need 4*tc. If the secondary cycle is a “Data Read”, then user could read the register content. See the following Figure 10-3 (2).

Note the Figure 6-5 to Figure 6-7 are use the 8080 MPU interface as examples.



(1) Command Write (Write Data to Register)



(2) Read Data from Register

Figure 10-3 : Command Write and Register Read Cycle

System Clock	Command Access Time
4MHz	1μs
6 MHz	667ns
8 MHz	500ns
10 MHz	400ns
12 MHz	333ns

10-4 Memory Write/Read

When users want to write data to memory – DDRAM or CGRAM, then a special Command cycle has to execute first, the register have to assign to “B0h” on Data Bus. Then the following Data Write cycle will write data into memory. If users want to read data from memory, then the register has to assign to “B1h” on Data Bus in Command Write cycle. Please see the following Figure 10-4 (1) and (2).

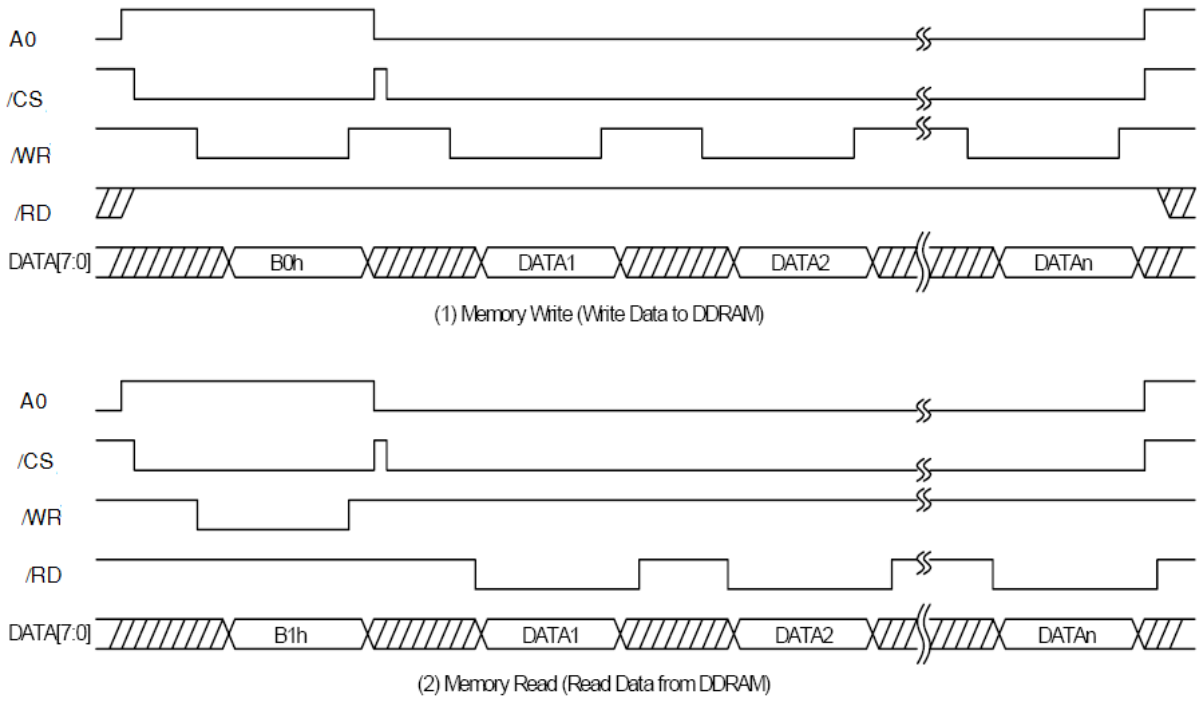


Figure 10-4 : Memory Write/Read Cycle

10-5 Status Read

RA8806 provides a dedicate Status Read cycle to help users know the status of RA8806. Please refer to following Figure 10-5 and the beginning of Section 13.0 “Register Description”.

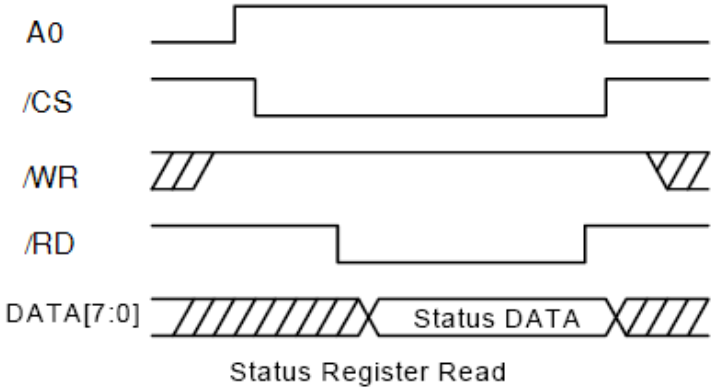


Figure 10-5 : Status Read Cycle

11. 0 BACKLIGHT CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Item	Symbol	Condition	Rating	Unit
Reverse Voltage	Vr		5	V
Absolute maximum forward current	Ifm		160	mA
Forward Current	If	Vf=5.0V	120	mA
Power Description	Pd		360	mW
Operating temperature range	Topr		-10~+60	^{0}C
Storage temperature range	Tst		-20~+70	^{0}C

11.2 ELECTRICAL/OPTLCAL CHARACTERISTICS

(Ta=25℃)

Item	Symbol	Min	Typ	Max	Unit	Condition
Forward Voltage	Vf	4.8	5.0	5.1	V	If=120mA
Reverse Current	Ir		120		uA	Vr=5 V
Dominant wave length	λp	--	--	--	nm	If=120mA
Spectral Line Half width	Δ λ		--			If=120 mA
Luminance	Lv		--		cd/m^2	If=120 mA
Color Coordinate	X		WHITE			If=120 mA
	Y					

12. 0 OPERATING PRINCIPLES & METHODS

12.1 DISPLAY WINDOW AND ACTIVE WINDOW

The RA8806 provides two windows for real application -- Display Window and Active Window. The Display Window is the actual resolution of LCD panel. Active is a sub-window in Display Window. The boundary of cursor shift depends on the active window. The relative registers of the two windows are as the following table.

Reg.	Bit_Num	Description	Reference
AWLR	Bit [5:0]	Define left boundary of the active window	REG[40h]
AWRR	Bit [5:0]	Define right boundary of the active window	REG[20h]
AWTR	Bit [7:0]	Define top boundary of the active window	REG[50h]
AWBR	Bit [7:0]	Define bottom boundary of the active window	REG[30h]
DWWR	Bit [5:0]	Define the width of the display window	REG[21h]
DWHR	Bit [5:0]	Define the height of the display window	REG[31h]

For RA8806, if LCD panel resolution is 320x240 pixels then the display window resolution is 320x240. We can create an active window in the display window like Figure 12-1. This figure show the display resolution is 320x240, and a 160x160 active window is on the upper-middle. The relative setting of the active window as following:

```
LCD_CmdWrite ( 0x40 ); // AWLR = 09h = 9 → ( 80 / 8) – 1
LCD_DataWrite ( 0x09 );
LCD_CmdWrite ( 0x20 ); // AWRR = 1Dh = 29 → ( 240 / 8 ) – 1
LCD_DataWrite ( 0x1D );
LCD_CmdWrite ( 0x50 ); // AWTR = 00h = 0
LCD_DataWrite ( 0x00 );
LCD_CmdWrite ( 0x30 ); // AWBR = 9Fh = 159 → 160 – 1
LCD_DataWrite ( 0x9F );
LCD_CmdWrite ( 0x40 ); // DWWR = 27h = 39 → ( 320 / 8 ) – 1
LCD_DataWrite ( 0x27 );
LCD_CmdWrite ( 0x40 ); // DWHR = EFh = 239 → 240 – 1
LCD_DataWrite ( 0xEF );
```

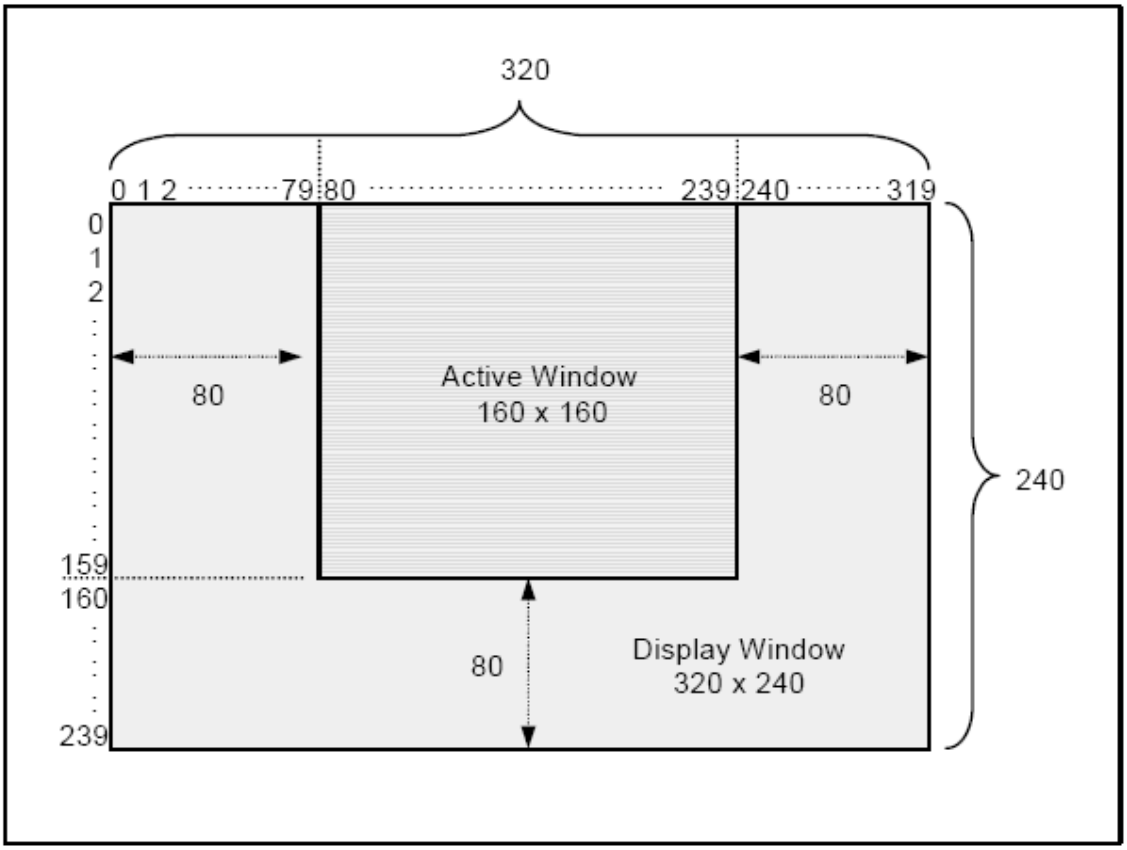


Figure 12-1: RA8806 Display Window and Active Window

12.2 IDLE TIME COUNTER (ITCR)

ITCR(REG[90h]) is used to determine the idle time during the LP peer-to-peer time. It has following meanings in function.

1. Adjusting the Frame Rate.(By extending the scan time of each COM)
2. Avoiding the generation of "Flicker".

The "Flicker" is generated by the violation of LCD scan cycle and Memory write cycle. "Flicker" means the noise of the scan data at such violation. By setting the ITCR, user can write the display memory only at "Idle" time to eliminate the "Flicker".

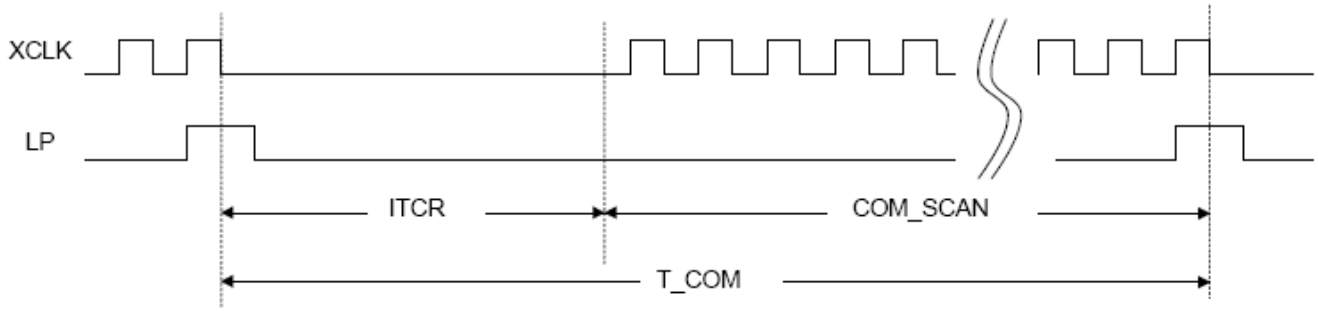


Figure 12-2: Idle Time Period

RA8806 scan time of each COM line can be calculated by the formulas.

COM_PRD = ((SEG_NO/LD_WIDTH) x (1 + EXT_MD)) ＋ ITCR) x XCK_PRD

In which the EXT_MD means extension mode is set or not, if REG[12h] Bit[6:4] = 110b/111b, EXT_MD = 1, or EXT_MD = 0. The "XCK_PRD" is one clock period of XCK. The XCK frequency is base on the system clock. It depends on the setting of Bit[3:2] of REG[MISC]. As to the Frame time and frame rate calculation. It would be:

FRM_PRD = COM_PRD x COM#

And

FRM_Rate = 1 / FRM_PRD

For example, when panel size is set to 320x240, system clock frequency is 8MHz, REG[MISC]Bit[3:2] = 10b, LCD driver data bus width is 4-bits, what the frame rate would be?

The System Clock(CLK) is 8MHz, and REG[MISC] Bit[3:2] = 10b → XCK = CLK/2, so the XCK_PRD is 250ns.

XCK_PRD = 1 / (CLK/2) = 1/4MHz = 250ns

COM_PRD = (320 / 4 ＋ ITCR) x XCK_PRD = (80+ ITCR) x 250(ns)

If the ITCR = A0h(160 in decimal):

COM_PRD **= (80+160) x 250ns = 240 x 250ns = 60μs**

The COM number is 240, so the frame period is:

FRM_PRD = 60μs x 240 = 14.4 ms

And the frame rate is:

Frame Rate = 1 / 10.8ms = 69.4 Hz

We can see the effect that the ITCR setting to the corresponding frame rate. So we can use it to adjust the frame rate. Please refer to Table 12-1. In that tables, we show some Frame Rate setting for difference resolution, system clock. But note the display quality is also depends on the module design and the material of liquid crystal.

Reg.	Bit_Num	Description	Reference
ITCR	Bit [7:0]	Define the idle time during the LP peer-to-peer time.	REG[90h]
MISC	Bit [3:2]	Select the clock frequency of XCK.	REG[01h]

Seg	Com	CLK (MHz)	XCK=CLK/2 REG[01h] Bit[3:2] = 10		XCK=CLK/4 REG[01h] Bit[3:2] = 01		XCK=CLK/8 REG[01h] Bit[3:2] = 00	
			Frame Rate (Hz)	REG[90h] ITCR	Frame Rate (Hz)	REG[90h] ITCR	Frame Rate (Hz)	REG[90h] ITCR
320	240	4	55	72	55	--	55	--
320	240	4	60	59	60	--	60	--
320	240	4	65	48	65	--	65	--
320	240	4	70	39	70	--	70	--
320	240	4	75	31	75	--	75	--
320	240	6	55	147	55	34	55	--
320	240	6	60	128	60	24	60	--
320	240	6	65	112	65	16	65	--
320	240	6	70	99	70	9	70	--
320	240	6	75	87	75	3	75	--
320	240	8	55	223	55	72	55	--
320	240	8	60	198	60	59	60	--
320	240	8	65	176	65	48	65	--
320	240	8	70	158	70	39	70	--
320	240	8	75	142	75	31	75	--
320	240	10	55	--	55	109	55	15
320	240	10	60	--	60	94	60	7
320	240	10	65	241	65	80	65	--
320	240	10	70	218	70	69	70	--
320	240	10	75	198	75	59	75	--
320	240	12	55	--	55	147	55	34
320	240	12	60	--	60	128	60	24
320	240	12	65	--	65	112	65	16
320	240	12	70	--	70	99	70	9
320	240	12	75	253	75	87	75	3

Table 12-1 : Frame Rate Table

12.3 RESET

The RA8806 requires a reset pulse at least 1024*tc long after power-on in order to re-initialize its internal state. If the oscillator frequency is 6Mhz, then the Reset pulse is at least 170.7μs. For maximum reliability, it is not recommended to apply a DC voltage to the LCD panel while the RA8806 is reset. Turn off the LCD power supplies for at least one frame period after the start of the reset pulse.

The RA8806 cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals XD, LP and FR are halted. A delay of 1ms (minimum) is required following the rising edges of both ZRST and VDD to allow for system stabilization. Please refer to Figure 12-3 for more detail description.

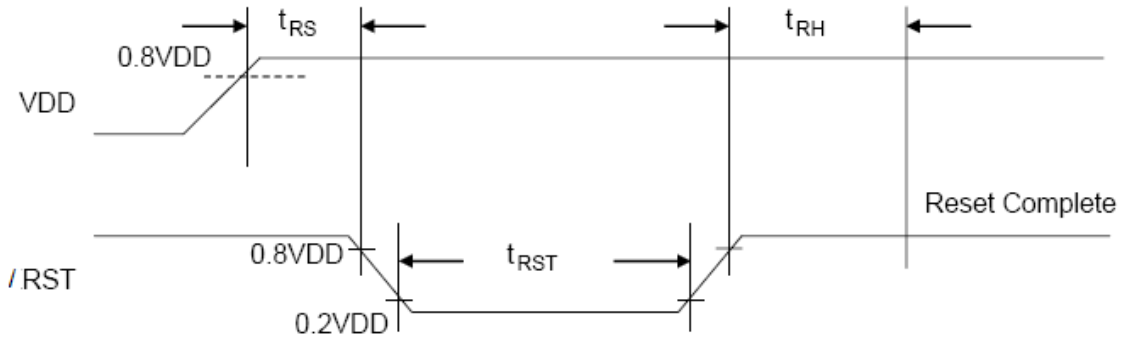


Figure 12-3: Reset Timing

Symbol	Description	Max.	Typ.	Min.	Unit
tRS	Reset setup time	--	--	1	ms
tRH	Reset hold time	--	--	1	ms
tRST	Reset active time	--	--	1024	tc (*)

*tC is the period of system clock,for example: 10MHz, tC = 100ns

12-4 Display Function

12-4-1 Character/Graphic Mode

There are two modes for MPU to write data to RA8806, i.e., character mode and graphic mode. In graphic mode, data is written directly to DDRAM in bit-map format. In character mode, data is written in code format, the font bit-map in the CGROM will be written to DDRAM by this way.

RA8806 stores two different sizes of characters in its font ROM - 1) half size font(8x16 pixels), 2) full size font(16x16). Figure 12-4 shows the examples.

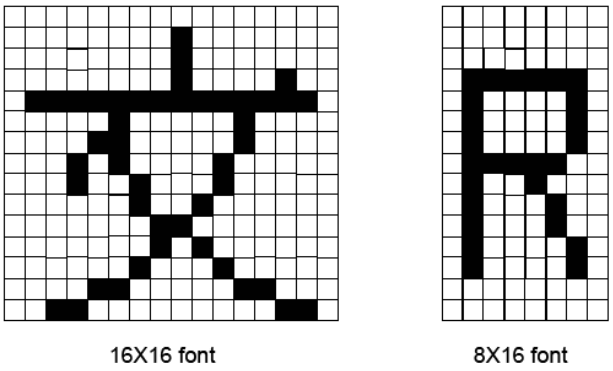


Figure 12-4: Full and Half Size Font

12-4-2 Graphic Display

The RA8806 graphics mode is use bit map to fill the data on the DDRAM. The Figure 12-5 is an example to show how to set graphics mode.

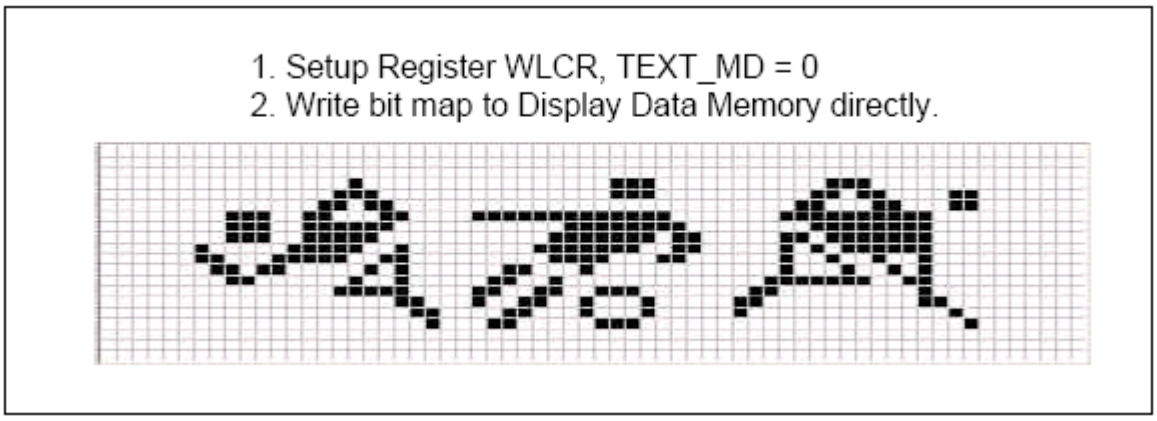


Figure 12-5 : Graphics Mode

The RA8806 support maximum resolution is 320x240 pixels, therefore it need 9.6Kbyte (320x240/8 = 9600) Display Data RAM(DDRAM) to store each pixel data. Figure 12-6 is an example to show the DDRAM data mapping to the LCD panel.

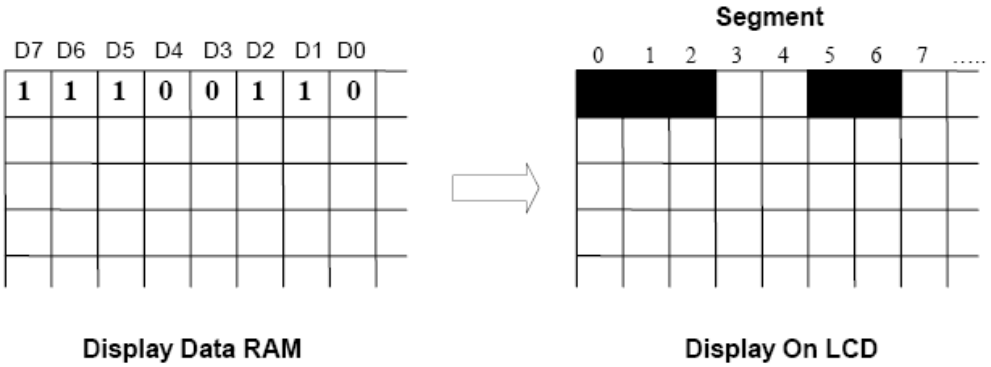


Figure 12-6: The Mapping of Display Data to LCD Panel

The RA8806 provide an Auto-Write feature to fill a data to all of the DDRAM. At first, user writes the data to Register PNTR then initials the Auto-Write function(Register FNCR Bit-3). RA8806 will fill the data to DDRAM in very short time. Normally this feature is used to clear screen or want to fill fixed pattern or background on screen.

12-4-3 Two Layer Display

The RA8806 embedded two DDRAM for two layers display. The register MAMR is used to show the visible display for DDRAM1 and DDRAM2. It provides six display modes:

Display DDRAM1
Display DDRAM2
Display DDRAM1 OR DDRAM2
Display DDRAM1 XOR DDRAM2
Display DDRAM1 NOR DDRAM2
Display DDRAM1 AND DDRAM2

Please refer Figure 12-7 and Register description of MAMR Bit[6:4] and Bit[3:2].

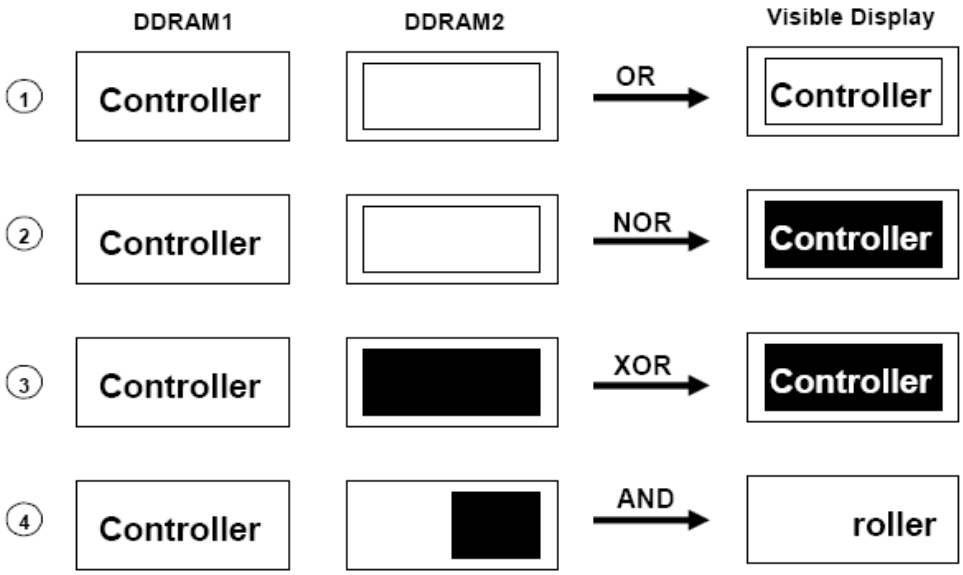


Figure 12-7 : Two Layers Display

Reg.	Bit_Num	Description	Reference
MAMR	Bit [6:4]	Display Layer Selection	REG[12h]
	Bit [3:2]	Two Layer Mode Selection	

In the past, if user wants to show the Chinese character has to in the graphics mode and use bit map data to fill the Chinese font one byte by one byte. But the RA8803 embedded hardware Chinese engine could accept two bytes Chinese BIG5 or GB code from MPU and show the character in text mode directly. Before the MPU pass 2bytes Chinese code to RA8803/8822, the user need to assign the cursor to the right position like traditional text mode. Because each Chinese code is 2byte, so if the MPU interface is use 8-bit then the MPU has to send twice(High byte and Low byte). If want to show English or numeric then MPU only need to send one byte ASCII code.

The RA8803 supports maximum 320x240 pixel resolution of display. Therefore the maximum full size character number at one page is 20x15, and half size character is 40x15.

12-4-4 Line Gap

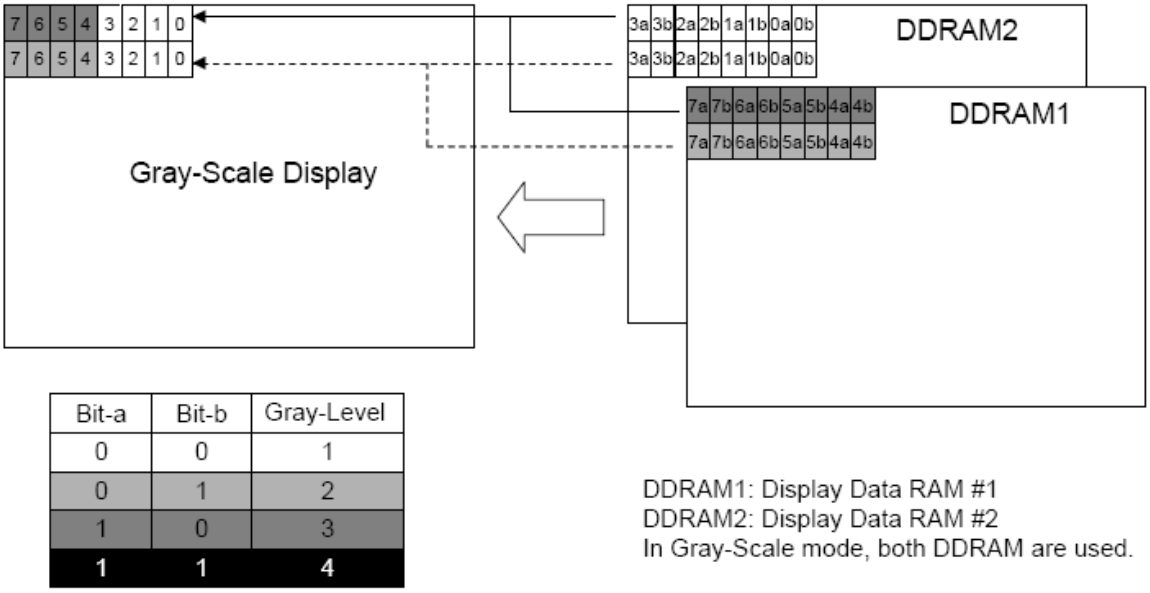
The RA8806 provide Line Gap feature. Especially in Chinese display, if add some space in each line will look better. The range of line gap is 1 ~ 16 pixel. Once the line gap is setup, the cursor will automatically move to property position for each line.

Setting the low nibble of the register CHWI, user can adjust the line gap. To deserve to be mentioned, when RA8806 operating in 90 degree mode, the line gap is either 0 pixel or 8 pixels, no matter what the font size. The selection of two conditions is according to Bit-3 of the register CHWI.

Reg.	Bit_Num	Description	Reference
CHWI	Bit [7:4]	Set Cursor Height	REG[11h]
	Bit [3:2]	Set Line Gap	

12-4-5 Gray Scale Display

The RA8806 also provide 4-gray-scale display implemented by FRC method. In gray level display mode, RA8806 combines the data of DDRAM1 and DDRAM2 as a gray picture. Each gray pixel occupies 2 bits of DDRAM data for display. Data [00b] indicate an empty pixel display and [11b] is solid display. [01b] & [10b] will be time sharing as 1/3 and 2/3 lightness. Please refer to Figure 12-8.



Bit-a	Bit-b	Gray-Level
0	0	1
0	1	2
1	0	3
1	1	4

Figure 12-7 : Mapping Rule of 4-Gray-Scale Display

According to the data write order, RA8806 support 2 data input methodology for Gray-Scale display. User can write the data as the same way of mono graphic display.

1. Horizontal moving first then Vertical
2. Vertical moving first then Horizontal

Reg.	Bit_Num	Description	Reference
MAMR	Bit 7	Cursor Auto Shifting Direction	REG[12h]
	Bit [6:4]	Gray Mode selection	

12-5 Eliminating Flicker Mode

RA8806 also provides “Eliminating Flicker Mode” in order to eliminate display errors at scan/MPU confliction. When the scan logic is processing scan task and at the same time the DDRAM is accessed by the MPU, the s can data will force to get a wrong one and may experience side effects such as “snow”. When the flicker or “snow” is too much, it will infect the display effect.

Therefore, RA8806 is designed to disable scan logic when MPU is accessing the DDRAM. And after it is completed, the scan logic active again. The “Eliminating Flicker Mode” separate Write and Read operating therefore no confliction will happen between scan logic and MPU cycle. That is, no data will lose. Ideally, it will have great improvement at display effect.

In the real application, sometimes the access method will cause a side effect for that the scan waveform of each row will vary by the MPU write cycle. The length of scan waveform for each row will different when data access frequently. In some condition, the display effect is poor. According to the real experiment result, we find that the display effect is perfect at graphic mode to use the “Eliminating Flicker Mode”. We suggest user can consider adapting it by their real application display effect.

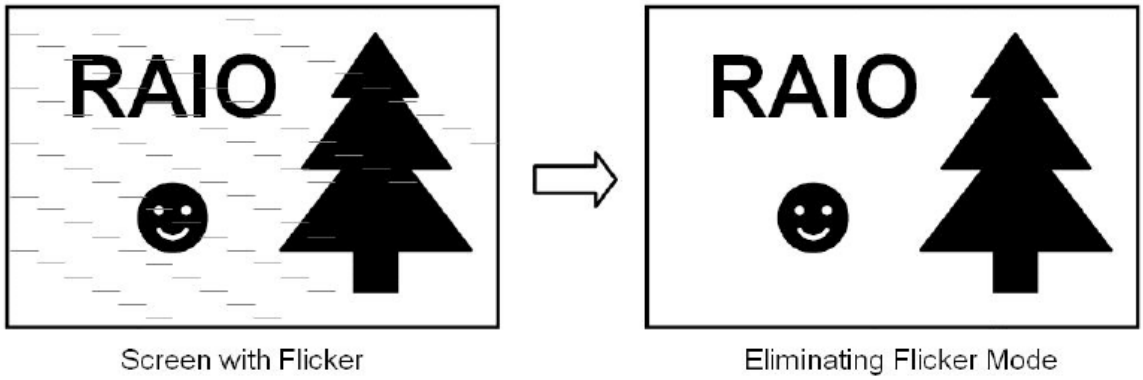


Figure 12-8 : Eliminating Flicker Mode

Reg.	Bit_Num	Description	Reference
MISC	Bit 7	The LCD Driver-Scan will auto-pending when busy.	REG[01h]

13. 0 REGISTER DESCRIPTION

13.1 REGISTER LIST TABLE

REG #	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def.
--	STATUS	MBUSY	SBUSY	SLEEP			WAKE_STS	KS_STS	TP_STS	--
00h	WLCR	PWR	LINEAR	SRST	--	TEXT_MD	ZDOFF	GBLK	GINV	00h
01h	MISC	NO_FLICKER	CLKO_SEL	BUSY_LEV	INT_LEV	XCK_SEL1	XCK_SEL0	SDIR	CDIR	04h
03h	ADSR	SCR_PEND	--	--	--	BIT_INV	SCR_DIR	SCR_HV	SCR_EN	00h
0Fh	INTR	--	WAKI_EN	KEYI_EN	TPI_EN	TP_ACT	WAK_STS	KEY_STS	TP_STS	00h
10h	WCCR	CUR_INC	FULL_OFS	BIT_REV	BOLD	T90DEG	CUR_EN	CUR_BLK	---	00h
11h	CHWI	CURH3	CURH2	CURH1	CURH0	ROWH3	ROWH 2	ROWH 1	ROWH 0	00h
12h	MAMR	CUR_HV	DISPMD2	DISPMD1	DISPMD0	L_MIX1	L_MIX 0	MW_MD1	MW_MD0	11h
20h	AWRR	--	--	AWR5	AWR4	AWR3	AWR2	AWR1	AWR0	27h
21h	DWWR	--	--	DWW5	DWW4	DWW3	DWW2	DWW1	DWW0	27h
30h	AWBR	AWB7	AWB6	AWB5	AWB4	AWB3	AWB2	AWB1	AWB0	EFh
31h	DWHR	DWH7	DWH6	DWH5	DWH4	DWH3	DWH2	DWH1	DWH0	EFh
40h	AWLR	--	--	AWL5	AWL4	AWL3	AWL2	AWL1	AWL0	00h
50h	AWTR	AWT7	AWT6	AWT5	AWT4	AWT3	AWT2	AWT1	AWT0	00h
60h	CURX	--	--	CURX5	CURX4	CURX3	CURX2	CURX1	CURX0	00h
61h	BGSG	--	--	BGSG5	BGSG4	BGSG3	BGSG2	BGSG1	BGSG0	00h
62h	EDSG	EDSG7	EDSG6	EDSG5	EDSG4	EDSG3	EDSG2	EDSG1	EDSG0	00h
70h	CURY	CURY7	CURY6	CURY5	CURY4	CURY3	CURY2	CURY1	CURY0	00h
71h	BGCM	BGCM7	BGCM6	BGCM5	BGCM4	BGCM3	BGCM2	BGCM1	BGCM0	00h
72h	EDCM	EDCM7	EDCM6	EDCM5	EDCM4	EDCM3	EDCM2	EDCM1	EDCM0	00h
80h	BTMR	BLKT7	BLKT6	BLKT5	BLKT4	BLKT3	BLKT2	BLKT1	BLKT0	00h
90h	ITCR	ITC7	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0	00h
A0h	KSCR1	KEY_EN	KEY4X8	KSAMP1	KSAMP0	LKEY_EN	KF2	KF1	KF0	00h

REG #	Name	D7	D6	D5	D4	D3	D2	D1	D0	Def.
A1h	KSCR2	KWAK_EN	--	--	--	LKEY_T1	LKEY_T0	KEYNO1	KEYNO0	00h
A2h	KSDR0	KSD07	KSD06	KSD05	KSD04	KSD03	KSD02	KSD01	KSD00	00h
A3h	KSDR1	KSD17	KSD16	KSD15	KSD14	KSD13	KSD12	KSD11	KSD10	00h
A4h	KSDR2	KSD27	KSD26	KSD25	KSD24	KSD23	KSD22	KSD21	KSD20	00h
B0h	MWCR	MWD7	MWD6	MWD5	MWD4	MWD3	MWD2	MWD1	MWD0	--
B1h	MRCR	MRD7	MRD6	MRD5	MRD4	MRD3	MRD2	MRD1	MRD0	--
C0h	TPCR1	TP_EN	TP_SMP2	TP_SMP1	TP_SMP0	TPWAK_EN	ACLK2	ACLK1	ACLK0	00h
C1h	TPXR	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C2h	TPYR	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
C3h	TPZR	TPX1	TPX0	--	--	TPY1	TPY0	--	--	00h
C4h	TPCR2	MTP_MD	--	--	--	--	--	MTP_PH1	MTP_PH2	00h
D0h	PCR	PWM_EN	PWM_DIS_LEV	--	--	PCLK_R3	PCLK_R2	PCLK_R1	PCLK_R0	00h
D1h	PDCR	PDUTY7	PDUTY6	PDUTY5	PDUTY4	PDUTY3	PDUTY2	PDUTY1	PDUTY0	00h
E0h	PNTR	PND7	PND6	PND5	PND4	PND3	PND2	PND1	PND0	00h
F0h	FNCR	ISO8859_EN	--	--	--	MCLR	ASC	ASC_SEL1	ASC_SEL0	00h
F1h	FVHT	FH1	FH0	FV1	FV0	--	--	--	--	00h

13.2 REGISTER DESCRIPTION

STATUS Register (A0 = 1, /WR = 1)

Bit	Description	Access
7	**Memory Write Busy Flag** 0 : Not busy. 1 : Busy, when font write or memory clear cycle is running, the busy flag = 1.	R
6	**SCAN_BUSY** 0 : Not busy. 1 : When driver scan logic is not idle(i.e. XCK is active), SCAN_BUSY = 1.	R
5	**SLEEP** 0 : Normal mode. 1 : Sleep mode.	R
4-3	NA	R
2	**Wakeup Status bit** (The same with REG[0Fh] Bit-2.)	R
1	**KS Status bit** (The same with REG[0Fh] Bit-1.)	R
0	**TP Status bit** (The same with REG[0Fh] Bit-0.)	R

REG [00h] Whole Chip LCD Controller Register (WLCR)

Bit	Description	Default	Access
7	**Power Mode** 0 : Normal Mode. All of the functions of RA8806 are available in this mode. 1 : Sleep Mode. When RA8806 is in Sleep mode, all of functions enter off mode, except the wake-up trigger block. If wake-up event occurred, RA8806 would wake-up and return to Normal mode.	0	R/W
6	**Linear Decode mode** This bit is used to define the Font ROM address mapping rule. The standard product is set to 0. And 1 for special application that when user a want to create a new Mask Code. 0 : BIG5/GB ROM mapping rule. 1 : User-defined ROM mapping rule.	0	R/W
5	**Software Reset** 0 : Normal Operation. 1 : Reset all registers except the contents of Display Data RAM (Only work at Normal mode). When this bit set to "1", the next MPU cycle for RA8806 have to wait 3 clocks at least.	0	R/W
4	Reserved	0	R
3	**Text Mode Selection** 0 : Graphical Mode. The written data will be treated as a bit-map pattern. 1 : Text Mode. The written data will be treated as an ASCII, BIG5 or GB code.	0	R/W
2	**Set Display On/Off Selection** The bit is used to control LCD Driver Interface signal – "DISP_OFF". 0 : DISP_OFF pin output low(Display Off). 1 : DISP_OFF pin output high(Display On).	0	R/W
1	**Blink Mode Selection** 0 : Normal Display. 1 : Blink Full Screen. The blink time is set by register BTMR.	0	R/W
0	**Inverse Mode Selection** 0 : Normal Display. 1 : Inverse Full Screen. It will cause the display inversed.	0	R/W

REG [01h] Misc. Register (MISC)

Bit	Description	Default	Access
7	**Eliminating Flicker** 1 : Eliminating flicker mode, scan will auto-pending when busy. 0 : Normal mode.	0	R/W
6	**Clock Output (Pin CLK_OUT) Control** 1 : The pin "CLK_OUT" indicates the SLEEP state of Status Register(0: Normal Mode, 1: Sleep Mode). 0 : The pin "CLK_OUT" is the output of Internal system clock.	0	R/W
5	**Busy Polarity (for "BUSY" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
4	**Interrupt Polarity (for "INT" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
3-2	**Driver Clock Selection** These two bits are used to select the clock frequency of XCK. 0 0 : XCK = CLK/8 0 1 : XCK = CLK/4 (Default) 1 0 : XCK = CLK/2 1 1 : XCK = CLK The "CLK" means system clock.	01	R/W
1	**SEG Scan Direction(SDIR)** 0 : SEG order is 0 ~ 319. 1 : SEG order is 319 ~ 0.	0	R/W
0	**COM Scan Direction(CDIR)** 0 : COM order 0 ~ 239. 1 : COM order 239 ~ 0.	0	R/W

REG [03h] Advance Display Setup Register (ADSR)

Bit	Description	Default	Access
7	**Scroll Function Pending** 1 : Scroll function pending 0 : Scroll function keep active Note: When SCR_HV(Bit-1) and SCR_EN(Bit-0) are changed, the function does not support.	0	R/W
6-4	Reserved	000	R
3	**BIT_ORDER(Set driver data output bit order)** 1 : Inverse driver output data order(Bit-7 to Bit-0, Bit-6 to Bit-1 and so on) 0 : Normal Mode	0	R/W

Bit	Description	Default	Access
2	**SCR_DIR(Scroll Direction)** When SCR_HV = 0(Horizontal Scroll) 0 : Left → Right. 1 : Right → Left. When SCR_HV = 1(Vertical Scroll) 0 : Top → Bottom. 1 : Bottom → Top.	0	R/W
1	**SCR_HV(Scroll Horizontal/Vertical)** 0 : Segment Scrolling(Horizontal). 1 : Common Scrolling(Vertical).	0	R/W
0	**SCR_EN(Scroll Enable)** 1 : Scroll function enable. 0 : Scroll function disable.	0	R/W

REG [0Fh] Interrupt Setup and Status Register (INTR)

Bit	Description	Default	Access
7	Reserved	0	R
6	**Wakeup Interrupt Mask** 1 : Enable wake-up Interrupt. 0 : Disable wake-up Interrupt.	0	R/W
5	**Key-Scan Interrupt Mask** 1 : Enable Key-Scan Interrupt. 0 : Disable Key-Scan Interrupt.	0	R/W
4	**Touch Panel Interrupt Mask** 1 : Generate interrupt output if touch panel was detected. 0 : Don't generate interrupt output if touch panel was detected.	0	R/W
3	**Touch Panel Event(Only activate in TP Manual mode)** 1 : Touch panel is touched. 0 : Touch panel is not touched.	0	R
2	**Wakeup Interrupt Status bit** 1 : Interrupt that indicate wake-up event happen from Sleep mode. 0 : No wake-up interrupt happen. User must write "0" to clear the Status bit.	0	R/W
1	**Key-Scan Interrupt Status bit** 1 : Key-Scan Detects Key Input. 0 : Key-Scan doesn't Detect Key Input. User must write "0" to clear the Status bit.	0	R/W
0	**Touch Panel Detect Status bit** 1 : Touch Panel Touched. 0 : Touch Panel Untouched. User must write "0" to clear the Status bit.	0	R/W

REG [10h] Whole Chip Cursor Control Register (WCCR)

Bit	Description	Default	Access
7	**CUR_INC** (Auto Increase Cursor Position in Reading/Writing DDRAM Operation.) 1 : Disable. 0 : Enable(Auto Increase).	0	R/W
6	**FULL_OFS** (Full-size and Half-size Character Alignment) 1 : Enable, in Full-size and Half-size character mixed mode. Chinese always start at full-size alignment. 0 : Disable.	0	R/W
5	**Reversed Data Write mode** 0 : Store Current Data to DDRAM Directly. 1 : Store Current Data to DDRAM Inversely.(i.e. 01101101Î 10010010)	0	R/W
4	**Bold Font** (Character Mode Only) 1 : Bold Font 0 : Normal Font	0	R/W
3	**Font Rotate mode**(T90DEG) 1 : Font rotates 90 degree. 0 : Normal font.	0	R/W
2	**Cursor Display** 1 : Set Cursor Display On. 0 : Set Cursor Display Off.	0	R/W
1	**Cursor Blinking** 1 : Blink Cursor. The blink time is determined by register BTMR. 0 : Normal.	0	R/W
0	Reserved	0	R

REG [11h] Cursor Height and Word Interval Register (CHWI)

Bit	Description	Default	Access
7-4	**Set Cursor Height** 0000 b → Height = 1 pixel. 0001 b → Height = 2 pixels. 0010 b → Height = 3 pixels. : 1111 b → Height = 16 pixels. Note: In normal font, the cursor width fixed to one byte(8 pixels). And cursor's height is from 1~16pixels that depends on Bit[7:4]. In vertical font, the cursor height fixed to 16 pixels, and width is from 1~8 pixels that depends on Bit[6:4].	0000	R/W

Bit	Description	Default	Access
3-0	**Set Line Gap** 0000 b → Gap = 1 pixel. 0001 b → Gap = 2 pixels. 0010 b → Gap = 3 pixels. : : 1111 b → Gap = 16 pixels.	0000	R/W

REG [12h] Memory Access Mode Register (MAMR)

Bit	Description	Default	Access
7	Cursor Auto Shifting Direction 0 : Cursor moves horizontally (left to right) first then vertically (top to down). 1 : Cursor moves vertically first then horizontally. Note: In graphic mode, the cursor moving is treated as unit of bytes in horizontal direction. At vertical direction, it's treated as unit of bit. At text mode, the bit is ignored, and the cursor moving is always in horizontal direction.	0	R/W
6-4	Display Layer and Display Mode Selection 0 0 0 : Gray Mode. In this mode, each pixel consists with 2 continuous bits in memory data. With the FRC methodology, 4-level-gray mode is implemented. The bit mapping is list as below. bit1 bit0 Gray --- 0 0 Level1 (Lightest) 0 1 Level2 1 0 Level3 1 1 Level4 (Darkest) Note: Gray mode doesn't support text-mode input. 0 0 1 : Show DDRAM1 data on screen. 0 1 0 : Show DRRAM2 data on screen. 0 1 1 : Show Two Layer Mode. The display rule depends on Bit-3 and Bit-2 as following. 1 0 X : NA. 1 1 0 : Extension Mode (1), the panel will show both DDRAM1 and DDRAM2 data on the screen. The RA8806 is available for 640x240 pixels panel. 1 1 1 : Extension Mode (2), the panel will show both DDRAM1 and DDRAM2 on the screen. The RA8806 is available for 320x480 pixels panel.	001	R/W

Bit	Description	Default	Access
3-2	Two Layer Mode Selection Combine the data of DDRAM1 and DDRAM2 on the screen when Bit[6:4] is set as "011". 0 0 : DDRAM1 "OR" DDRAM2. 0 1 : DDRAM1 "XOR" DDRAM2. 1 0 : DDRAM1 "NOR" DDRAM2. 1 1 : DDRAM1 "AND" DDRAM2.	00	R/W
1-0	MPU Read/Write Layer Selection 0 0 : Access CGRAM.(512Byte) 0 1 : Access DDRAM1. 1 0 : Access DDRAM2. 1 1 : Access both DDRAM1 and DDRAM2 concurrently	01	R/W

REG [20h] Active Window Right Register (AWRR)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Active Window Right Position → Segment-Right** Note: AWRR must be equal or larger then AWLR, and less or equal then the value 27h (40 in decimal).	27h	R/W

REG [21h] Display Window Width Register (DWWR)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Set Display Window Width Position → Segment-Width** **Segment-Right = (Segment Number / 8) – 1** If LCD panel resolution is 320x240, the value of the register is: (320 / 8) - 1 = 39 = 27h	27h	R/W

REG [30h] Active Window Bottom Register (AWBR)

Bit	Description	Default	Access
7-0	**Active Window Bottom Position → Common-Bottom** Note: AWBR must be equal or larger then AWTR, and less or equal then the value EFh(239 in decimal)	EFh	R/W

REG [31h] Display Window Height Register (DWHR)

Bit	Description	Default	Access
7-0	**Display Window Height Position → Common- Height** **Common_ Height = LCD Common Number –1** If LCD panel resolution is 320x240, the value of the register is: 240 – 1 = 239 = EFh	EFh	R/W

REG [40h] Active Window Left Register (AWLR)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Active Window Left Position → Segment-Left** Note: AWLR must be equal or less then AWRR, and less then the value 27h(39 in decimal)	00h	R/W

REG [50h] Active Window Top Register (AWTR)

Bit	Description	Default	Access
7-0	**Active Window Top Position → Common-Top** Note: AWTR must be equal or less then AWBR, and less then the value EFh (239 in decimal)	00h	R/W

Note:

REG[20h, 30h, 40h, and 50h] are used to dominate an active window for line/row changing when writing data. Users can use these four registers to set the left/right/top/bottom boundary of active window. When data goes beyond the right boundary of it, the cursor will automatically change the next line to write data. It will move to the left boundary of new line in active window. When the data comes to the right-bottom corner, the next write will cause the cursor to move to the left-top corner.

REG[21h, 31h] are used to set Display Window Resolution. Users can set the viewing scope of Display Data RAM. Column width (DWWR) of RA8806 can be set between 0h ~ 27h, and Row height (DWHR) can be set between 0h ~ EFh.

REG [60h] Cursor Position X Register (CURX)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Cursor Position of Segment / RAM0 Address[4:0]** Define the cursor address of segment, a value from 0h ~ 27h(0 ~ 40 in decimal) When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[4:0] is the address for writing bit-map data. When create a full-size font, normally set to 0. When create an odd half-size font, normally set to 0, and set 10h for even font.	00h	R/W

REG [61h] Begin Segment Position Register of Scrolling (BGSG)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Segment Start Position of Scrolling Mode** REG[61h] defines the start position (left boundary) of scroll window, it must be a value that less or equal to the REG[62h], which defines the end position(right boundary) of scroll window. Also it must be less then the value of 27h (40 in decimal), for the Display Data RAM limit.	00h	R/W

REG [62h] End Segment Position Register of Scrolling (EDSG)

Bit	Description	Default	Access
7-6	Reserved	00	R
5-0	**Segment End Position of Scrolling Mode** REG[62h] defines the end position(right boundary) of scroll window, it must be a value that larger or equal to the REG[61h], which defines the end position(left boundary) of scroll window. Also it must be less or equal then the value of 27h(40 in decimal), for the Display Data RAM limit.	00h	R/W

REG [70h] Cursor Position Y Register (CURY)

Bit	Description	Default	Access
7-0	**Cursor Position of Common / RAM0 Address[8:5]** Define the cursor address of common, a value from 0h ~ EFh(0 ~ 239 in decimal). When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[3:0] is indicate which font will be created. And Bit[7:4] are not available.	00h	R/W

REG [71h] Scrolling Action Range Begin Common Register (BGCM)

Bit	Description	Default	Access
7-0	**Common Start Position of Scrolling Mode** REG[71h] defines the begin position(top boundary) of scroll window, it must be a value that less or equal to the REG[72h], which defines the end position(bottom boundary) of scroll window. Also it must be less then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

REG [72h] Scrolling Action Range END Common Register (EDCM)

Bit	Description	Default	Access
7-0	**Common Ending Position of Scrolling Mode** REG[72h] defines the end position(bottom boundary) of scroll window, it must be a value that larger or equal to the REG[71h], which defines the end position(top boundary) of scroll window. Also it must be less or equal then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

Note:

REG[61h, 62h, 71h, 72h] dominate a named scroll window for scroll function. They must be set before the scroll function is enable.

REG [80h] Blink Time Register (BTMR)

Bit	Description	Default	Access
7-0	**Cursor Blink Time and Scroll Time** **Blinking Time = Bit[7:0] x (Frame width)** **Frame width = 1/Frame Rate** The Frame Rate is depends on the DWWR and DWHR and ITCR setting.	00h	R/W

Notes:

1. The Setting also determines the scroll moving speed.
2. The Frame width is the time that the controller scan whole panel, it depends on the system clock frequency, setting of display window, driver interface (4-bits/8-bits), Idle time (ITCR), and dual mode or gray scale mode, etc.

REG [90h] Idle Time Counter Register (ITCR)

Bit	Description	Default	Access
7-0	**Idle Time Setting, in count of system clock**. The value can determine the scan time of each COM of the LCD. **COM_PRD = (COM_SCAN + ITCR) x XCK_PRD** In which, **COM_SCAN = (SEG_NO/LD_WIDTH) x (1 + EXT_MD)** **XCK_PRD = 1 / XCK** **COM_PRD:** The finally scan period for each COM(Unit : ns). **COM_SCAN:** The really scan time for each COM. **XCK_PRD:** One cycle time of XCK. XCK is depends on the system clock (CLK) and REG[01h] Bit[3:2]. If system clock is 8MHz, REG[01h] Bit[3:2] = 10b, then XCK_PRD = 250ns. **SEG_NO:** Segment number, i.e. 240x160 panel, SEG_NO = 240. **EXT_MD:** In extension mode1 or 2(REG[12h] Bit[6:4] = 111b or 110b), the EXT_MD = 1, otherwise EXT_MD = 0. **LD_WIDTH:** Driver data width. If LCD driver data bus is 4-bits then LD_WIDTH = 4. If LCD driver data bus is 8-bits then LD_WIDTH = 8.	00h	R/W

REG [A0h] Key-Scan Control Register 1 (KSCR1)

Bit	Description	Default	Access
7	**Key-Scan Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6	**Key-Scan Matrix Selection** 1 : 4x8 Matrix(KOUT[3:0] is used, KOUT[7:4] please keep floating) 0 : 8x8 Matrix(KOUT[7:0] is used)	0	R/W

Bit	Description	Default	Access
5-4	**Key-Scan Data Sampling Times** De-bounce times of scan frequency. 0 0 : 4 0 1 : 8 1 0 : 16 1 1 : 32	00	R/W
3	**LNGKEY_EN : Long Time Key Function Enable** LNGKEY_EN = 0 ： Long key function is disable. LNGKEY_EN = 1 ： Long key function is enable.	0	R/W
2-0	**KF2-0: Key-Scan frequency.** If system clock is 10MHz, then the related Key-Scan timing are as following:	000	R/W

KF2	KF1	KF0	Key-Scan Pulse Width (KOUT period)	Key-Scan Cycle (4x8)	Key-Scan Cycle (8x8)
0	0	0	16μs	64μs	128μs
0	0	1	32μs	128μs	256μs
0	1	0	64μs	256μs	512μs
0	1	1	128μs	512μs	1.024ms
1	0	0	256μs	1.024ms	2.048ms
1	0	1	512μs	2.048ms	4.096ms
1	1	0	1.024ms	4.096ms	8.192ms
1	1	1	2.048ms	8.192ms	16.384ms

REG [A1h] Key-Scan Controller Register 2(KSCR2)

Bit	Description	Default	Access
7	Key-Scan Wakeup Function Enable Bit 0: Key-Scan Wakeup function is disable. 1: KEY-SCAN Wakeup function is enable.	0	R/W
6-4	Reserved	000	R
3-2	Long Key Timing Adjustment 00 : About 0.625sec(for 8MHz Clock source) 01 : About 1.25sec(for 8MHz Clock source) 10 : About 1.875 sec(for 8MHz Clock source) 11 : About 2.5 sec(for 8MHz Clock source)	00	R/W
1-0	Numbers of Key Hit. 00 : No key is pressed 01 : One key is pressed, read REG[A2h] for the key number. 10 : Two key is pressed, read REG[A2h ~ A3h] for the key number. 11 : Three key is pressed, read REG[A2h ~ A4h] for the key number.	00	R

REG [A2h ~ A4h] Key-Scan Data Register (KSDR0 ~ 2)

Bit	Description	Default	Access
7-0	Key Strobe Data The corresponding key number that is pressed.	00h	R

REG [B0h] Memory Write Command Register (MWCR)

Bit	Description	Default	Access
7-0	**Memory data write command from the cursor position.** Note: Write memory data, user must write the MWCR command first, then write DATA cycle.	NA	R/W

REG [B1h] Memory Read Command Register (MRCR)

Bit	Description	Default	Access
7-0	**Memory data read command from the cursor position.** Note: Memory read cycle in text mode, the cursor move in same behavior like graphic mode. B1h will perform a pre-read function. So the cursor position will increase after the MRCR command is write.	NA	R/W

REG [C0h] Touch Panel Control Register 1 (TPCR1)

Bit	Description	Default	Access
7	**Touch Panel Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6-4	**TP Sample Time Adjusting** 000 : Wait 50μs for ADC data ready. 001 : Wait 100μs for ADC data ready. 010 : Wait 200μs for ADC data ready. 011 : Wait 400μs for ADC data ready. 100 : Wait 800μs for ADC data ready. 101 : Wait 1.6ms for ADC data ready. 110 : Wait 3.2ms for ADC data ready. 111 : Wait 6.4ms for ADC data ready. Note: When touch panel detects the Touch event, to avoid the signal instability, the sampled time is delayed to wait the signal stable. Here time calculation is the example of system clock 10MHz.	000	R/W
3	**Touch Panel Wake-up Enable** 1: Touch panel can wake-up the Sleep mode (At the condition that ADC is enabled). 0 : Disable the touch panel wake-up function	0	R/W

Bit	Description	Default	Access
2-0	**ADC Clock Convert Speed** 0 0 0 : CLK / 4 0 0 1 : CLK / 8 0 1 0 : CLK /16 0 1 1 : CLK / 32 1 0 0 : CLK / 64 1 0 1 : CLK / 128 1 1 0 : CLK / 256 1 1 1 : CLK / 512 The "CLK" means system clock.	000	R/W

REG [C1h] Touch Panel X High Byte Data Register (TPXR)

Bit	Description	Default	Access
7-0	**Touch Panel X Data Bit[9:2](Segment)**	00h	R

REG [C2h] Touch Panel Y High Byte Data Register (TPYR)

Bit	Description	Default	Access
7-0	**Touch Panel Y Data Bit[9:2] (Common)**	00h	R

REG [C3h] Touch Panel Segment/Common Low Byte Data Register (TPZR)

Bit	Description	Default	Access
7-4	Reserved	0000	R
3-2	**Touch Panel Y Data Bit[1:0] (Common)**	00	R
1-0	**Touch Panel X Data Bit[1:0] (Segment)**	00	R

REG [C4h] Touch Panel Control Register 2 (TPCR2)

Bit	Description	Default	Access
7	**TP Manual Mode Enable** 1 : Using the manual mode. 0 : Auto mode.	0	R/W
6-2	Reserved	00h	R
1-0	**Mode selection for TP Manual Mode** 00: IDLE mode: ADC idles. 01: Wait for TP event, touch panel event could cause the interrupt or be read from REG[0Fh] B3. 10: Latch X data, in the phase, X Data can be latched in REG[C1h] and REG[C3h]. 11: Latch Y data, in the phase, Y Data can be latched in REG[C2h] and REG[C3h].	00	R/W

REG [D0h] PWM Control Register (PCR)

Bit	Description	Default	Access
7	**PWM enable** 1 : Enable 0 : Disable, PWM_OUT level depends on the REG[D0h] Bit-6.	0	R/W
6	**PWM Disable Level** 0 : PWM_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM_OUT is Normal H when PWM disable or Sleep mode.	0	R/W
5-4	Reserved	00	R
3-0	**PWM Clock Source Divide Ratio** 0000 b ： CLK / 1 0001 b ： CLK / 2 0010 b ： CLK / 4 0011 b ： CLK / 8 : : 1111 b ： CLK / 32768 The “CLK” means system clock. For example, CLK is 8MHz: 0000 b ： PWM clock source = 8MHz, 0001 b ： PWM clock source = 4MHz, : : 1111 b ： PWM clock source = 256Hz.	0000	R/W

REG [D1h] PWM Duty Cycle Register (PDCR)

Bit	Description	Default	Access
7-0	**PWM Cycle Duty Selection Bit** 00h ： 1 / 256 01h ： 2 / 256 High period 02h ： 3 / 256 High period : : FFh ： 256 / 256 High period	0	R/W

REG [E0h] Pattern Data Register (PNTR)

Bit	Description	Default	Access
7-0	**Data Written to DDRAM(Display Data RAM)** The pattern that will be filled to active window in memory clear function. When REG[F0h] Bit-3 is ‘1’, the data in the REG[E0h] will be filled to the whole active window.	00h	R/W

REG [F0h] Font Control Register (FNCR)

Bit	Description	Default	Access
7	**ISO8859 Mode** 0 : Disable. The contents of ASCII block 1 ~ 4 are show as Table C-1~ Table C-4 of Appendix B. 1 : Enable. The ASCII block 1 ~ 4 indicate the ISO8859-1 ~ 4 standard and show as Table C-5 ~ Table C-8 of Appendix C.	0	R/W
6-4	Reserved	000	R
3	**Memory Clear Function Write Function** 0 : No Action. 1 : Memory clear function active, fill the data of FNTR to Active window. When this bit is set to "1", RA8806 will automatically read PNTR data, and fill it to Active window (Range: [AWLR, AWTR] ~ [AWRR, AWBR]), after clear completed, this bit will be cleaned to "0".	0	R/W
2	**ASCII Mode Enable** 1 : All input data will be decoded as ASCII (00h ~ FFh) 0 : In text mode (REG[00h] Bit-3), the RA8806 will check the first written byte data first. If less then 80h then it's treated as ASCII (Half-size). Or it's treated as a full-size text(GB, BIG5 or User-created font).	0	R/W
1-0	**ASCII Blocks Select** 0 0 : Map to ASCII block 1. (Table C-1 and Table C-5 of Appendix C.) 0 1 : Map to ASCII block 2. (Table C-2 and Table C-6 of Appendix C.) 1 0 : Map to ASCII block 3. (Table C-3 and Table C-7 of Appendix C.) 1 1 : Map to ASCII block 4. (Table C-4 and Table C-8 of Appendix C.)	00	R/W

REG [F1h] Font Size Control Register (FVHT)

Bit	Description	Default	Access
7-6	**Set Character Horizontal Size** 0 0 : One Time of normal font width. 0 1 : Two Times of normal font width. 1 0 : Three Times of normal font width. 1 1 : Four Times of normal font width.	00	R/W
5-4	**Set Character Vertical Size** 0 0 : One Time of normal font height. 0 1 : Two Times of normal font height. 1 0 : Three Times of normal font height. 1 1 : Four Times of normal font height.	00	R/W
3-0	Reserved	0000	R

14. 0 QUALITY GUARANTEE

14.1 ACCEPTABLE QUALITY LEVEL

Inspection items	Sampling procedures	AQL
Visual-operating (Electro-optical)	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	0.65
Visual-not operating	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5
Dimension measurement	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5

14.2 Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

- Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

- Driving voltage

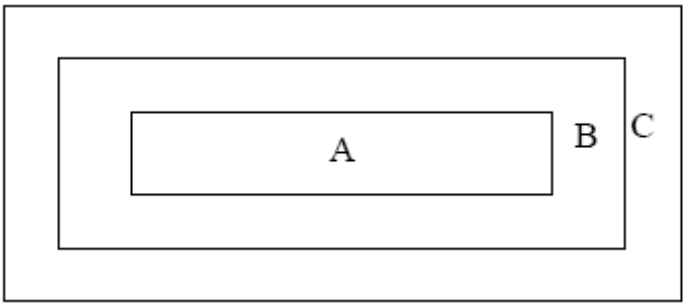
The V0 value which the most optimal contrast can be obtained near the specified V0 in the specification. (Within ±0.5V of the typical value at 25℃.).

14.3 Definition of inspection zone in LCD

Zone A: character/Digit area

Zone B: viewing area except Zone A (ZoneA + ZoneB =minimum Viewing area)

Zone C: Outside viewing area (invisible area after assembly in customer's product)



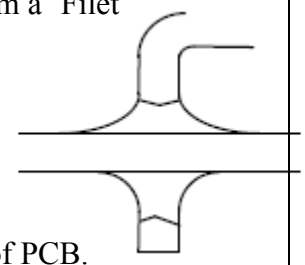
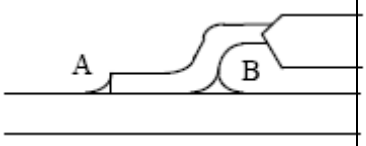
Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

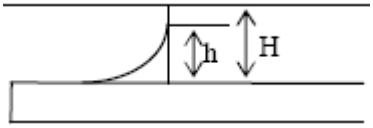
14.4 Inspection Standard

- **Major Defect**

Item No	Items to be inspected	Inspection Standard	Classification of defects
1	All functional defects	1) No display 2) Display abnormally 3) Missing vertical，horizontal segment 4) Short circuit 5) Back-light no lighting, flickering and abnormal lighting.	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed.	

- **Module Cosmetic Criteria**

No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (∅0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ∅0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a ‘Filet’ all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side (In case of ‘Through Hole PCB’) Solder to reach the Components side of PCB. 	Minor
	2. Flat packages	Either ‘Toe’ (A) or ‘Seal’ (B) of the lead to be covered by ‘Filet’. Lead form to be assume over solder. 	Minor

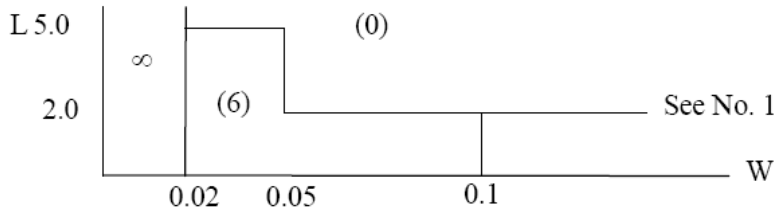
No.	Item	Judgment Criterion	Partition
8	3. Chips	(3/2) H ≥ h ≥ (1/2) H 	Minor

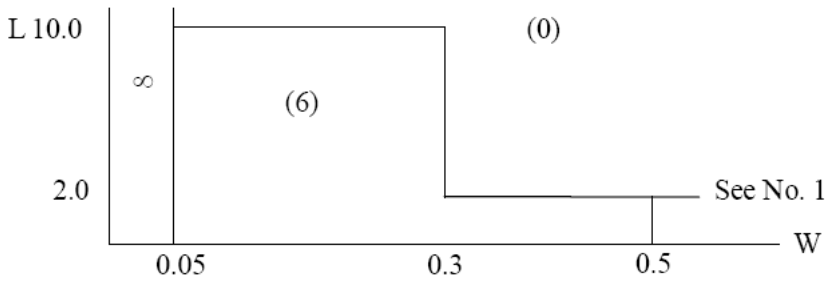
● Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition
1	Spots	In accordance with *Screen Cosmetic Criteria (Operating) No.1*.	Minor
2	Lines	In accordance with *Screen Cosmetic Criteria (Operating) No.2*.	Minor
3	Bubbles in polarizer	<table><tr><td>Size : d</td><td>mm</td><td>Acceptable Qty in active area</td></tr><tr><td>d</td><td>≤ 0.3</td><td>Disregard</td></tr><tr><td>0.3 < d</td><td>≤ 1.0</td><td>3</td></tr><tr><td>1.0 < d</td><td>≤ 1.5</td><td>1</td></tr><tr><td>1.5 < d</td><td></td><td>0</td></tr></table>	Minor
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor
7	Contamination	Not to be noticeable.	Minor

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating)

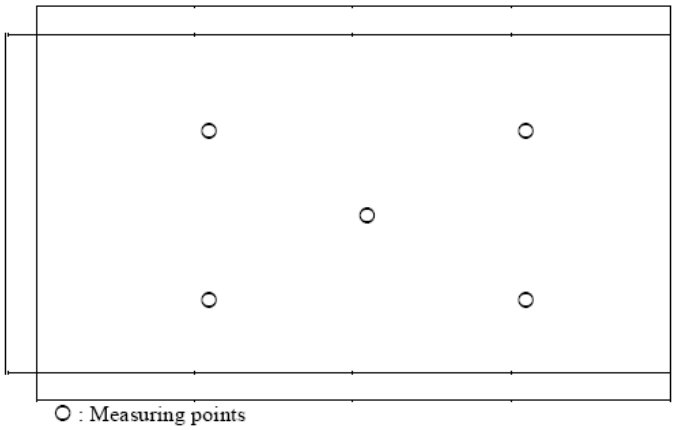
<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.1</td><td>Disregard</td></tr>
<tr><td>0.1 < d ≤ 0.2</td><td>6</td></tr>
<tr><td>0.2 < d ≤ 0.3</td><td>2</td></tr>
<tr><td>0.3 < d</td><td>0</td></tr>
</table>
Note : Including pin holes and defective dots which must be within one pixel size.
B) Unclear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.2</td><td>Disregard</td></tr>
<tr><td>0.2 < d ≤ 0.5</td><td>6</td></tr>
<tr><td>0.5 < d ≤ 0.7</td><td>2</td></tr>
<tr><td>0.7 < d</td><td>0</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>A) Clear
 

Note :
( ) - Acceptable Qty in active area
L - Length (mm)
W - Width (mm)
∞ - Disregard
B) Unclear
 

‘Clear’ = The shade and size are not changed by Vop.
‘Unclear’ = The shade and size are changed by Vop.</td><td>Minor</td></tr>
</table>

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	Minor
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as pot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤ 2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  	Minor

Note :

(1) The limit samples for each item have priority.

(2) Complex defects are defined item by item, but if the numbers of defects are defined in above table, the total number should not exceed 10.

(3) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allowed. Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of Æ5mm.
- 10 or over defects in circle of Æ10mm.
- 20 or over defects in circle of Æ20mm.

15. 0 RELIABILITY

15.1 Content of Reliability Test

No.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage	+80℃±2℃/200 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.missing segments; 5.Glass crack; 6. Current Idd is twice higher than initial value.
2	Low Temperature Storage	-30℃±2℃/200 hours	
3	High Temperature Operating	+70℃±2℃/120 hours	
4	Low Temperature Operating	-20℃±2℃/120 hours	
5	Temperature Cycle	-20℃±2℃~25~70℃±2℃×10cycles (30min.) (5min.) (30min.)	
6	High Temperature / Humidity operation	50℃±5℃×90%RH/120 hours	
7	Vibration Test	Frequency ： 10Hz~55Hz~10Hz Amplitude： 1.5mm, X， Y， Z direction for total 3hours (Packing condition)	
8	Drooping test	Drop to the ground from 1m height, one time, and every side of carton. (Packing condition)	
9	Static electricity test	Voltage:±8KV R: 330Ω C: 150pF Air discharge, 10time	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

16. 0 PRECAUTIONS FOR USING LCD MODULES

16.1 Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketone
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

16.2 Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

16.3 Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

17. 0 USING LCD MODULES

17.1 About Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

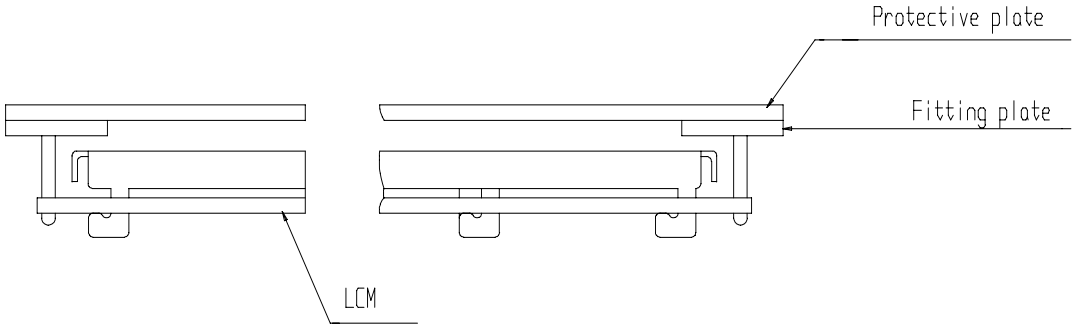
(9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinate to the polarizer).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

17.2 Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

17.3 Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutation of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

17.4 Soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280°C ± 10°C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

17.5 Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (V0). Adjust V0 to show the best contrast.

(2) Driving the LCD in the voltage above the limit shortens its life.

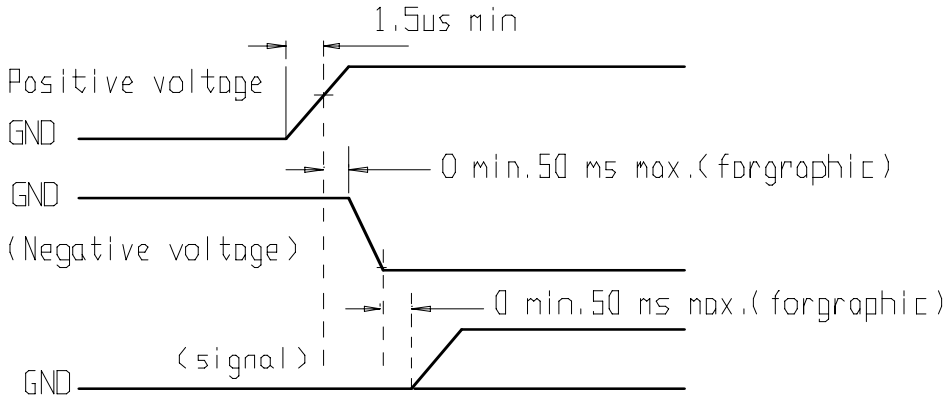
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit.

Therefore, it must be used under the relative condition of 40°C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



17.6 Storage

When storing LCDs as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for desiccant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

(4) Environmental conditions :

- Do not leave them for more than 168hrs. at 60°C.
- Should not be left for more than 48hrs. at -20°C.

17.7 Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

17.8 Limited Warranty

Unless agreed between HYDISPLAY and customer, HYDISPLAY will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with HYDISPLAY LCD/LCM acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to HYDISPLAY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of HYDISPLAY limited to repair and/or replacement on the terms set forth above. HYDISPLAY will not be responsible for any subsequent or consequential events.

17.9 Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet, conductors and terminals.

18. 0 APPENDIX

18.1 Initialization Code

```
void LCD_CmdWrite(uchar regnada)
{

    LCD_RD = 1;
    LCD_A0 = 1;
    LCD_CS =0; //Chip enable.

    DATA_PORT = regnada;
    LCD_WR = 0;
    LCD_WR = 1;

    LCD_CS =1; //Chip disable.
}

void LCD_DataWrite(uchar wrdata)
{
    LCD_RD = 1;
    LCD_A0 = 0;
    LCD_CS =0; //Chip enable.

    DATA_PORT = wrdata;
    LCD_WR = 0;
    LCD_WR = 1;

    LCD_CS =1; //Chip disable.
}

void WriteDataToREG(uchar regname,uchar regdata)
{
    LCD_CmdWrite(regname);
    LCD_DataWrite(regdata);
}
```

```
//RA8806 Initialization
void LCD_Initial(void)
{
    WriteDataToREG(0x00,0x00);//WLCR
    WriteDataToREG(0x01,0x04);//MISC XCK=CLK/4 @6MHz;

    WriteDataToREG(0x03,0x83);//ADSR
    WriteDataToREG(0x0F,0x00);//INTR
    WriteDataToREG(0x10,0x00);//WCCR

    WriteDataToREG(0x11,0x00);//CHWI
    WriteDataToREG(0x12,0x11);//MAMR

    WriteDataToREG(0x20,0x27);//AWRR
    WriteDataToREG(0x21,0x27);//DWRR
    WriteDataToREG(0x30,0xEF);//AWBR
    WriteDataToREG(0x31,0xEF);//DWHR
    WriteDataToREG(0x40,0x00);//AWLR
    WriteDataToREG(0x50,0x00);//AWTR

    WriteDataToREG(0x60,0x00);//CURX
    WriteDataToREG(0x61,0x00);//BGSG
    WriteDataToREG(0x62,0x00);//EDSG

    WriteDataToREG(0x70,0x00);//CURY
    WriteDataToREG(0x71,0x00);//BGCM
    WriteDataToREG(0x72,0x00);//EDCM

    WriteDataToREG(0x80,0x00);//BTMR
    WriteDataToREG(0x90,9); //ITCR
    WriteDataToREG(0xA0,0x40);//KSCR1
    WriteDataToREG(0xA1,0x00);//KSCR2

    WriteDataToREG(0xC0,0x00);//TPCR1

    WriteDataToREG(0xD0,0x00);//PCR
    WriteDataToREG(0xD1,0x00);//PDCR

    WriteDataToREG(0xE0,0x00);//PNTR
    WriteDataToREG(0xF0,0x00);//FNCR
    WriteDataToREG(0xF1,0x00);//FVNT
}
```

18.2 Power Supply Circuit Diagram